The European Design Platform

Challenges and Opportunities for Open-Source EDA

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EUROPEAN PARTNERSHIP

1. Chips JU: Chips for Europe initiative and ECS R&I

2. The European Design Platform & the role of open-source EDA/IP

3. Looking ahead: Challenges and opportunities for open-source EDA

EUROPEAN PARTNERSHIP

What is the Chips Joint Undertaking?

Chips JU is a tri-partite public-private partnership, established in September 2023, in an amendment to the Single Basic Act, to implement the first pillar of the Chips Act.

Chips JU continues the activities of its predecessors in the field of electronic components and systems (ECS), aiming to advance nano-electronic chip technologies in Europe, promoting digital sovereignty, digitalisation, and environmental responsibility.

European Union
European Commission

Public Authorities
Participating States

Private Members
Industry Associations

TRI-PARTITE STRUCTURE

The European Chips Act

European Semiconductor Board (Governance)

Pillar 1: Chips for Europe Initiative

- Initiative on infrastructure building in synergy with the EU's research programmes
- Support to start-ups and SMEs

Pillar 2: Security of Supply

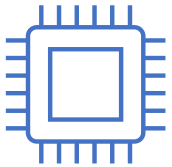
- First-of-a-kind semiconductor production facilities

Pillar 3: Monitoring & Crisis Response

- Monitoring and alerting
- Crisis coordination mechanism with MS
- Strong Commission powers in times of crisis

European Chips Act Objective 1

build up and maintain a virtual design platform, available across the Union, integrating existing and new design facilities with extended libraries and electronic design automation (EDA) tools;



extend the design capabilities by fostering innovative developments, such as open-source processor architectures and other innovative architectures, chiplets, programmable chips, new types of memory, processors, accelerators or low power chips, that are built in accordance with security-by-design principles;

ECS R&I Calls

Innovation along the entire value chain

- Focus topics covering AI, cybersecurity, high-performance computing (HPC), semiconductors, and more.
- Chips Joint Undertaking is aligning global research initiatives with European priorities.
- Chips JU is bridging together industry, academia, and policymakers for impactful results.
- It enables large-scale projects with EU and international investment.
- € **1.3 billion**

Chips for Europe Initiative

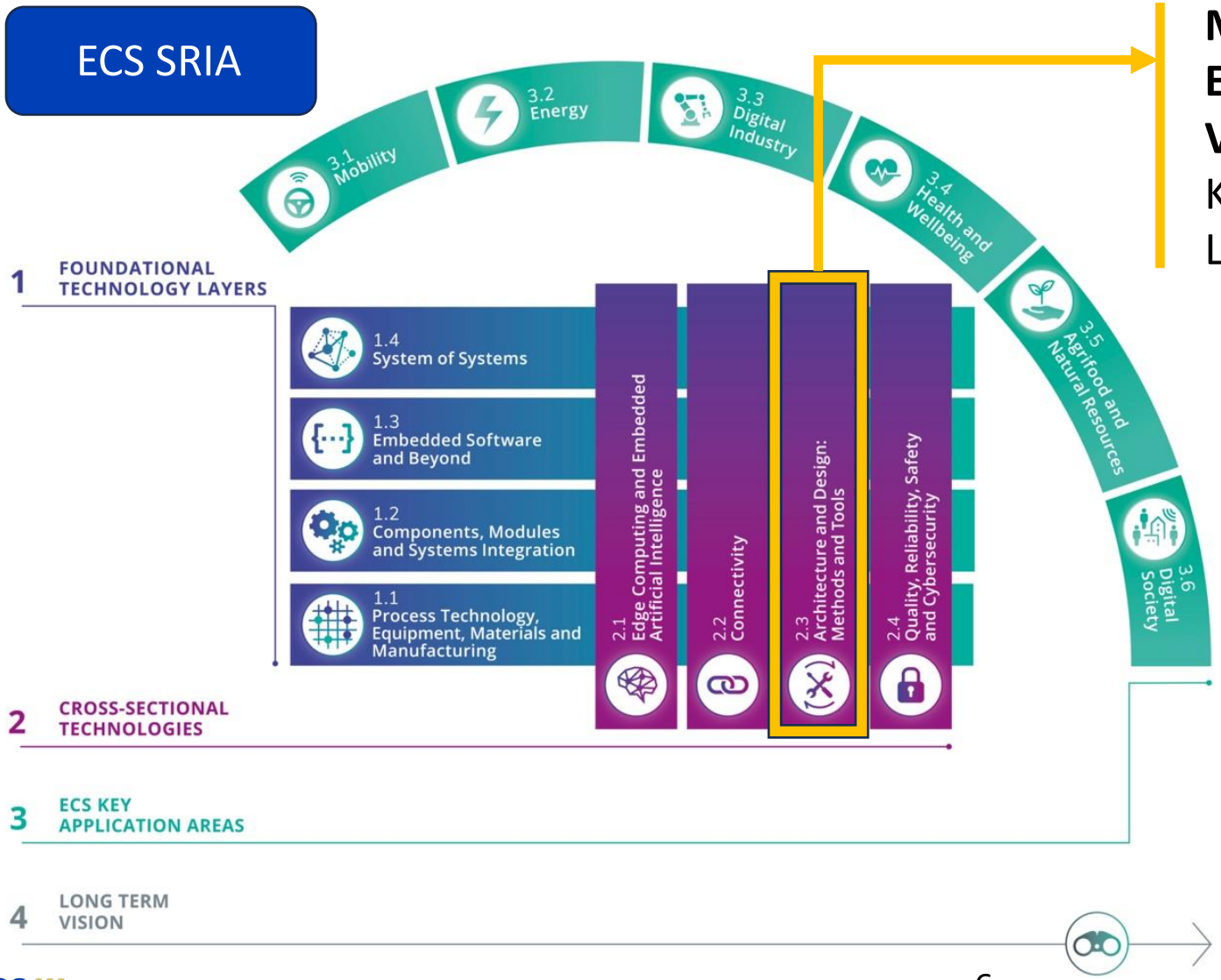
Capacity Building through the Chips Act

- **Chips Act:** one of Europe's largest industrial policies aimed at increasing Europe's share of global chip production.
- Chips JU implements the main part of the first pillar of the Chips Act, the **Chips for Europe Initiative**.
- Chips JU acts as a facilitator for public-private partnerships, ensuring that the necessary funding is directed toward strategic projects.
- It aligns the goals of the EU, its Member States, and the private sector. This **tri-partite structure** enables coordinated efforts in semiconductor innovation and capacity building in Europe.
- € **2.8 billion**

EUROPEAN PARTNERSHIP

ECS R&I Calls

Innovation along the entire value chain



Major Challenge 1:
Enabling cost- and effort-efficient Design and Validation Frameworks for High-Quality ECS
Key focus area:
Lifecycle-aware holistic design flows.

Appendix A: Roadmap Open Source HW/SW and RISC-V based IP blocks
"there is a need for high quality open source EDA tools supporting industrial-grade open source IP cores"

ECS R&I Calls

Innovation along the entire value chain: Focus Topics on RISC-V

TRISTAN (2021)	Development of open-source RISC-V building blocks • Focus on industrialising open-source tools for RISC-V
ISOLDE (2022)	Design of Customisable and Domain Specific Open-source RISC-V Processors • Focus on interoperability between open-source and proprietary EDA to achieve high-performance cores
Rigoletto (2024)	High Performance RISC-V Automotive Processors supporting SDV • Focus on open hardware platform and EDA tools for automotive

TURANDOT (call 2025, in GAP): design framework tailored for RISC-V-based automotive systems

ECS R&I Calls

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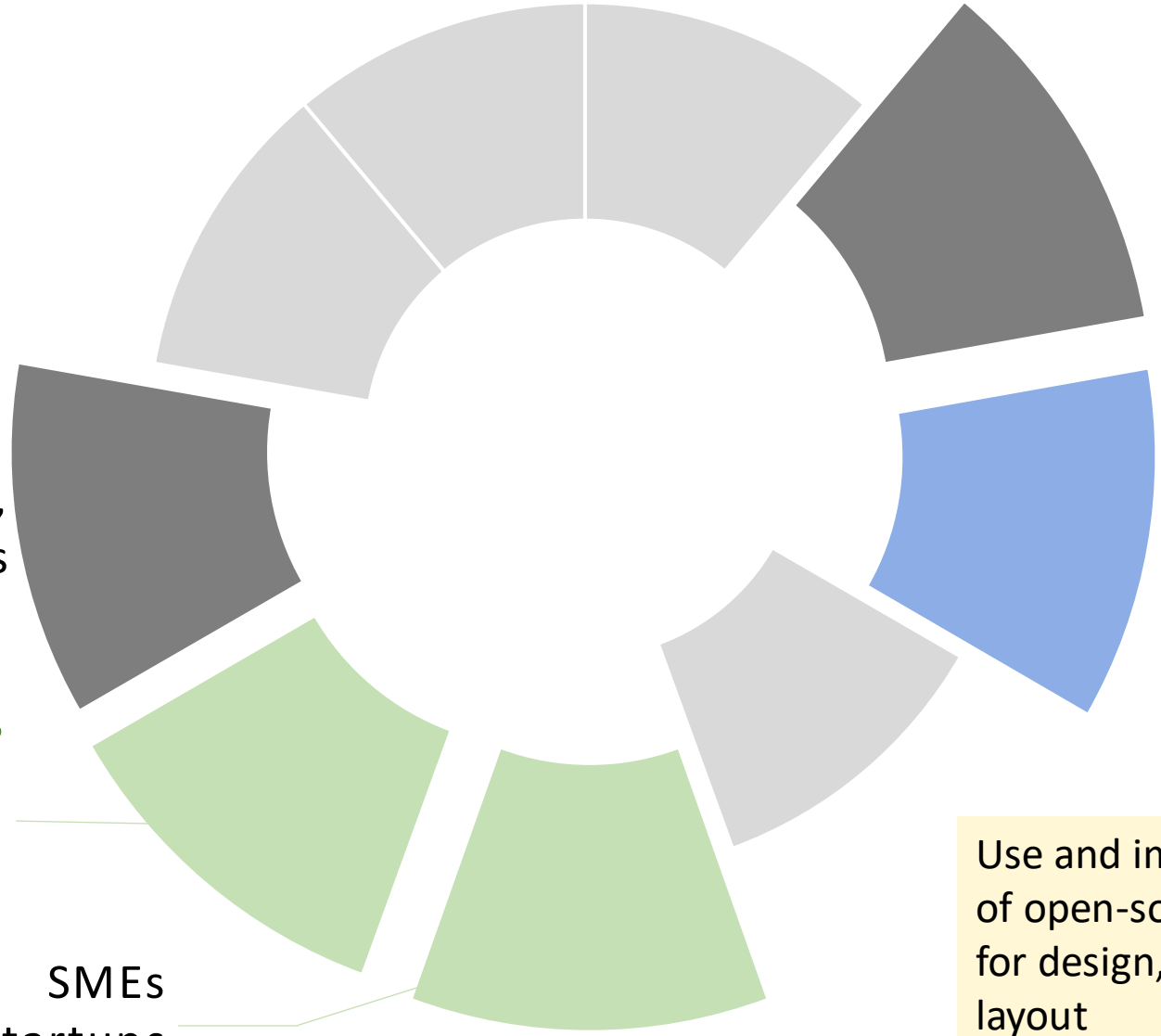
Chips for Europe Initiative

Capacity Building through the Chips Act

Pilot Lines



Manufacturers

Fabs, Packaging, Testing

Pilot Lines

NanoIc, FAMES, APECS, WBG, PIXEurope

Suppliers

Equipment, materials, services, tools

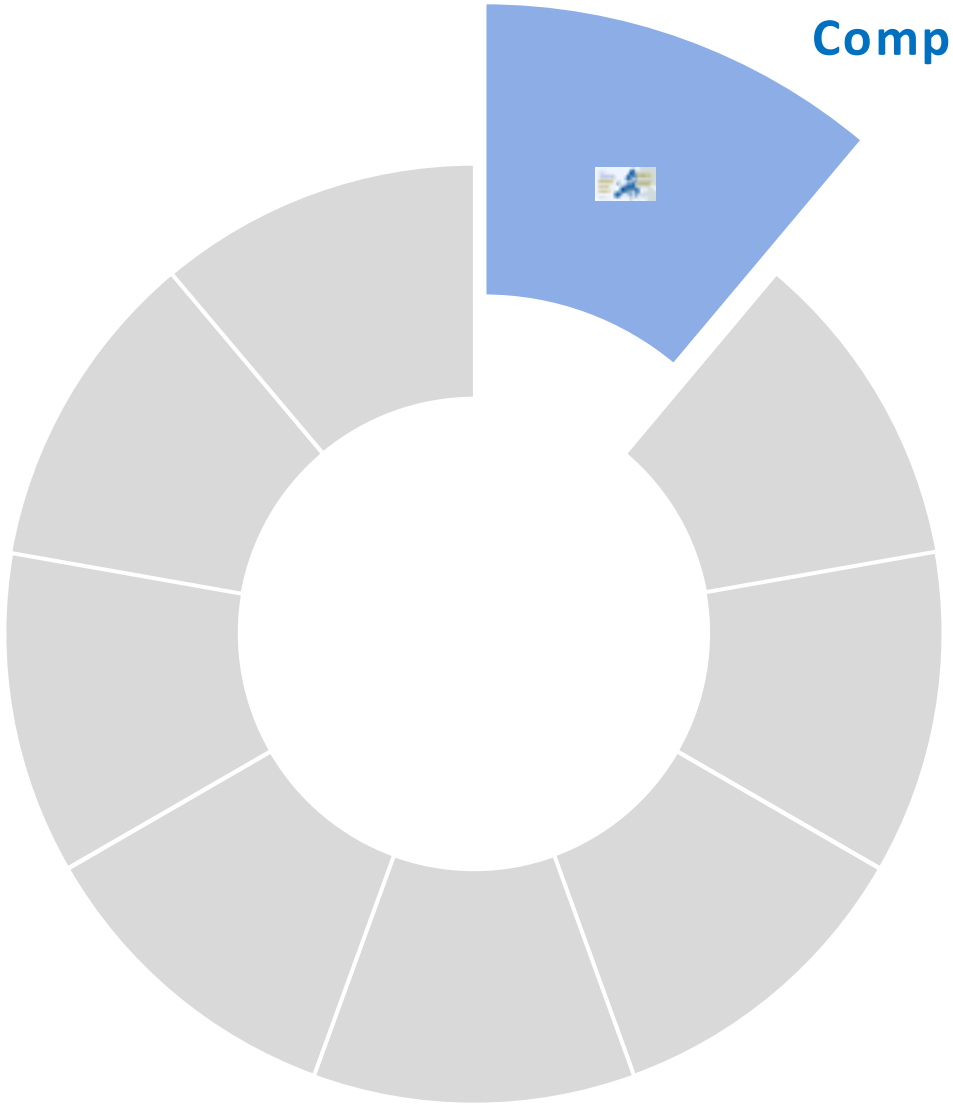
Users

System houses
RTOs
IDMs

SMEs
Startups

Use and improvement of open-source tools for design, simulation, layout

Competence Centres



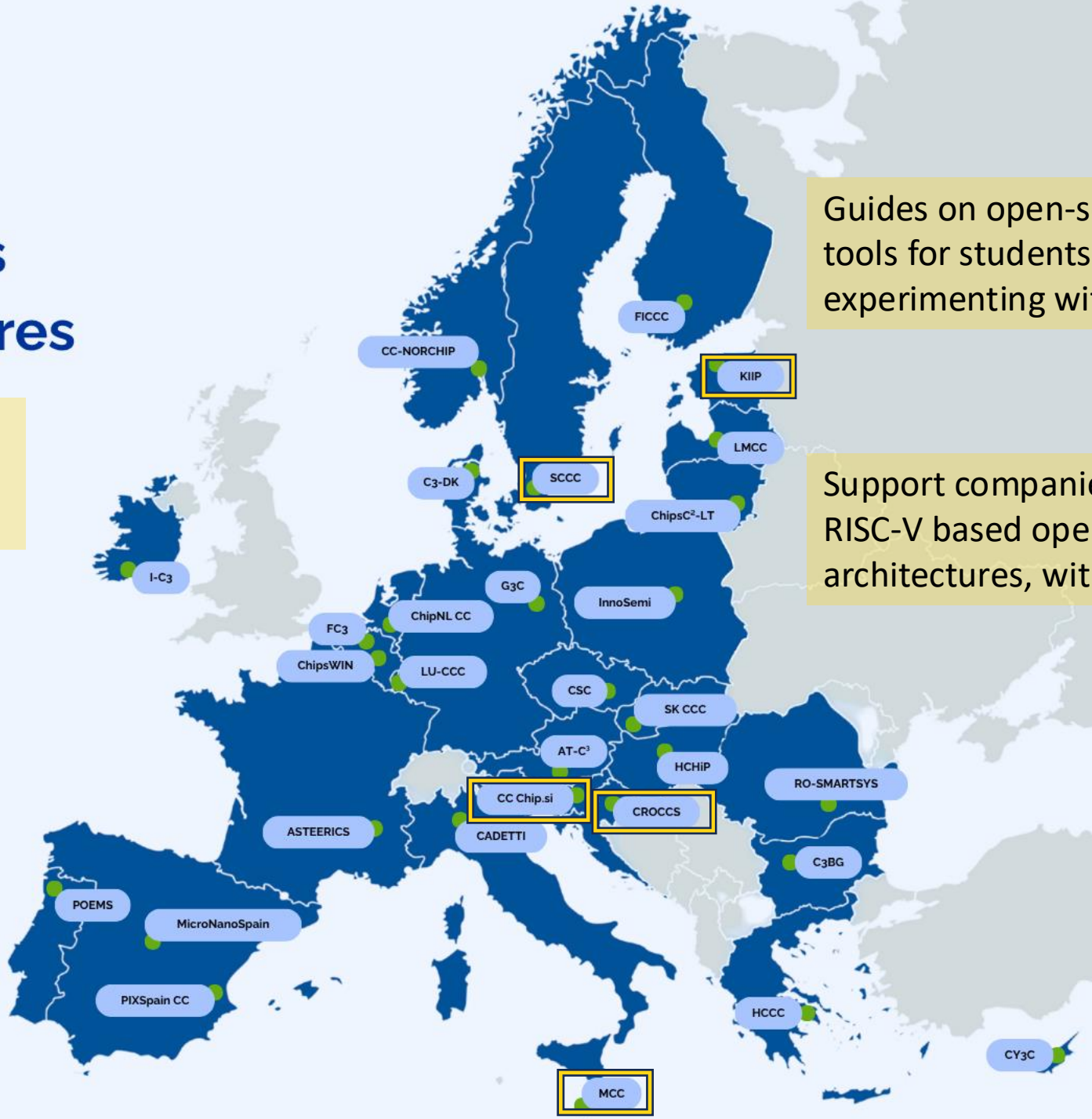
aCCCess

30 European Chips Competence Centres

Workshops on open-source EDA tools, High-Level Synthesis, and RISC-V bare-metal programming

Seminar on chip design using open-source EDA

Training modules with open-source tooling and IP



Guides on open-source EDA tools for students experimenting with chip design

Support companies in designing RISC-V based open-source architectures, with open EDA

linkedin.com/company/aCCCess

Quantum actions

Chips JU call 2026 on Quantum Chips Design:
Developing and promoting interoperability standards and shared reference architectures for quantum chip design workflows, possibly also ***open-source development****.*

CHAMP-ION:
PDKs based on open-source EDA

Quantum actions

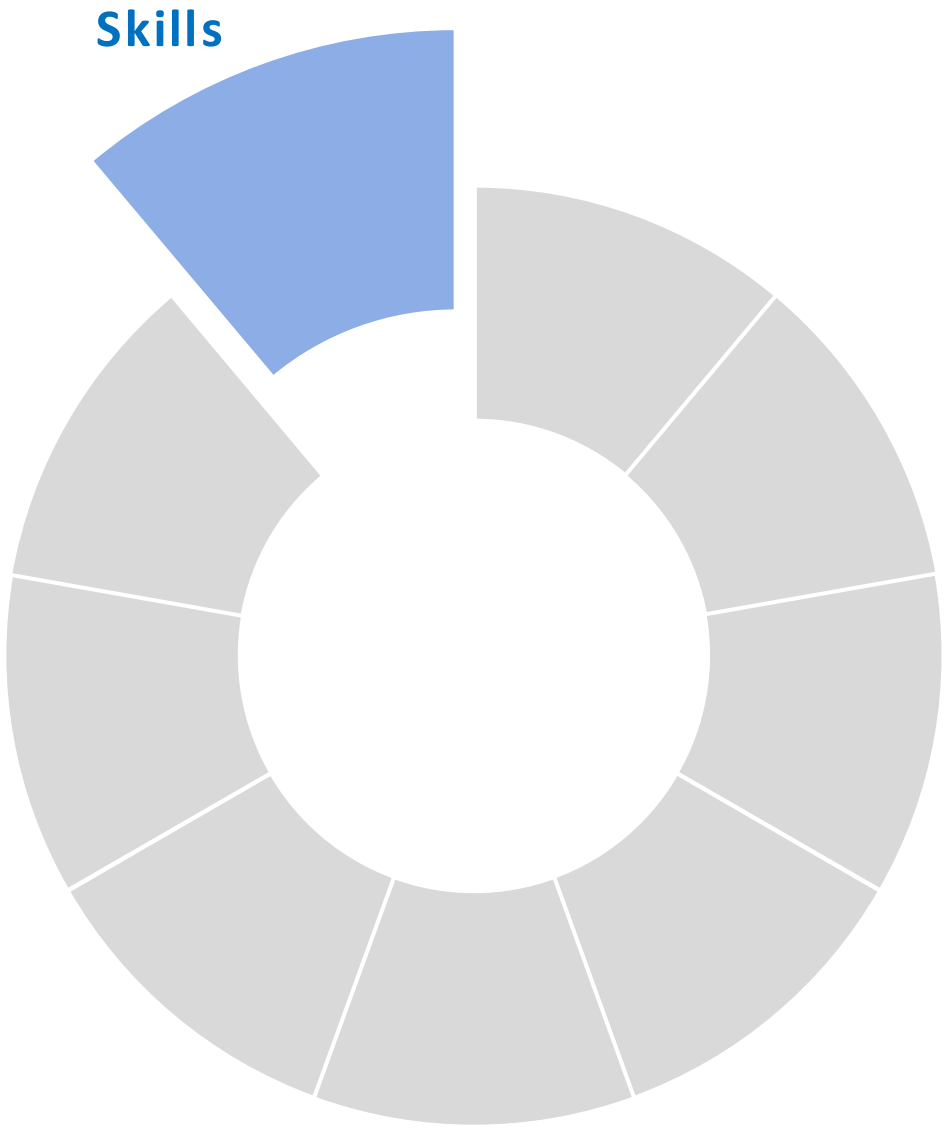
Superconducting
Semiconducting
Photonics
Diamond-based
Neutral-atoms
Trapped Ions

Skills

Chips JU call 2026 on Stimulation of Chip Design:

*Strong collaboration with the **Open-Source EDA** projects stemming from the HORIZON-JU-Chips-2025-IA-EDA call to ensure easy access to and use of the developed open source tools in these calls.*

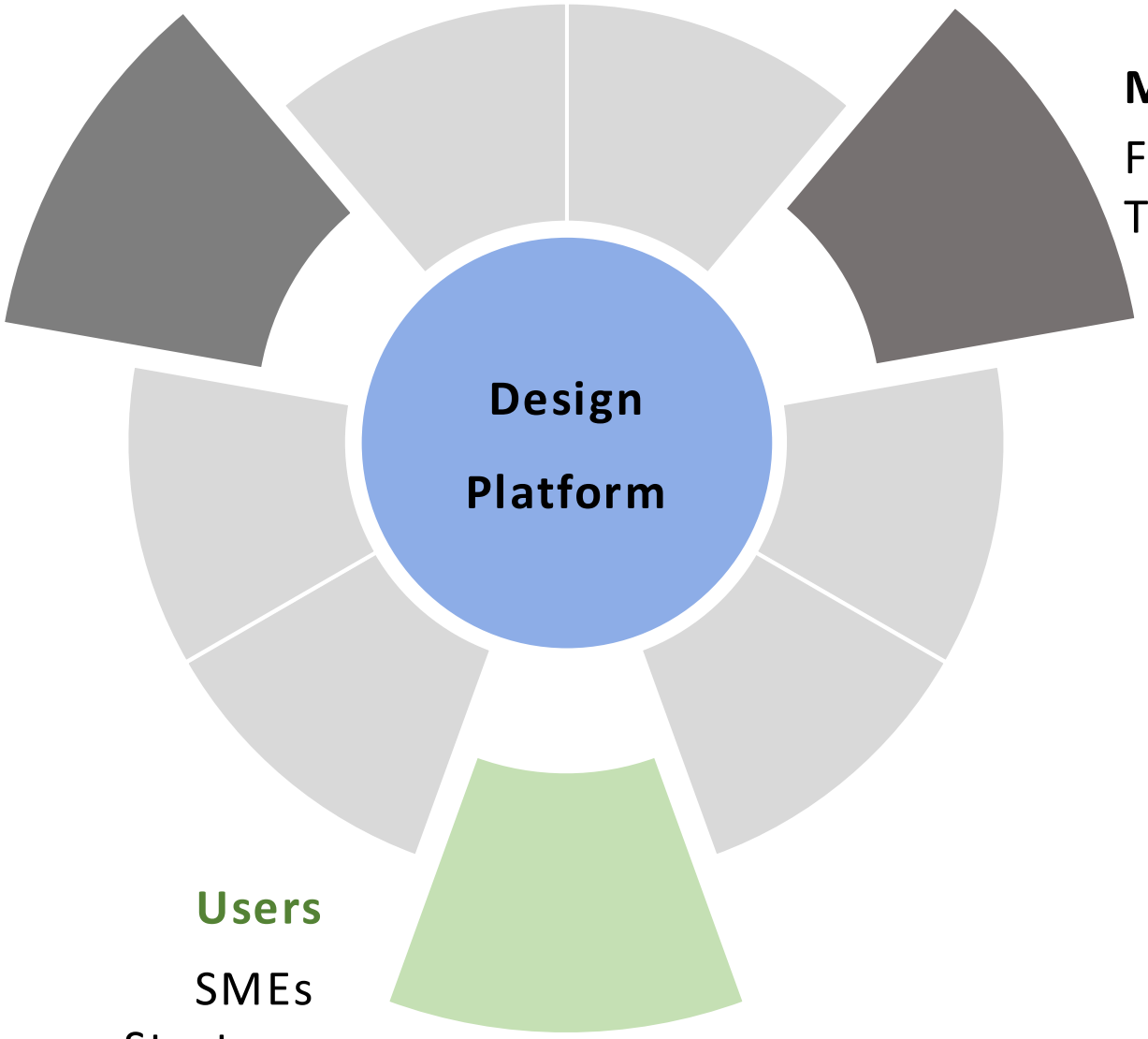
*User-friendly **open-source digital design flows and starter kits** for undergraduate and high-school settings.*



Design Platform

Suppliers

EDA, Tools, Services



Manufacturers

Fabs, Packaging, Testing

Users

SMEs
Startups

Design Platform

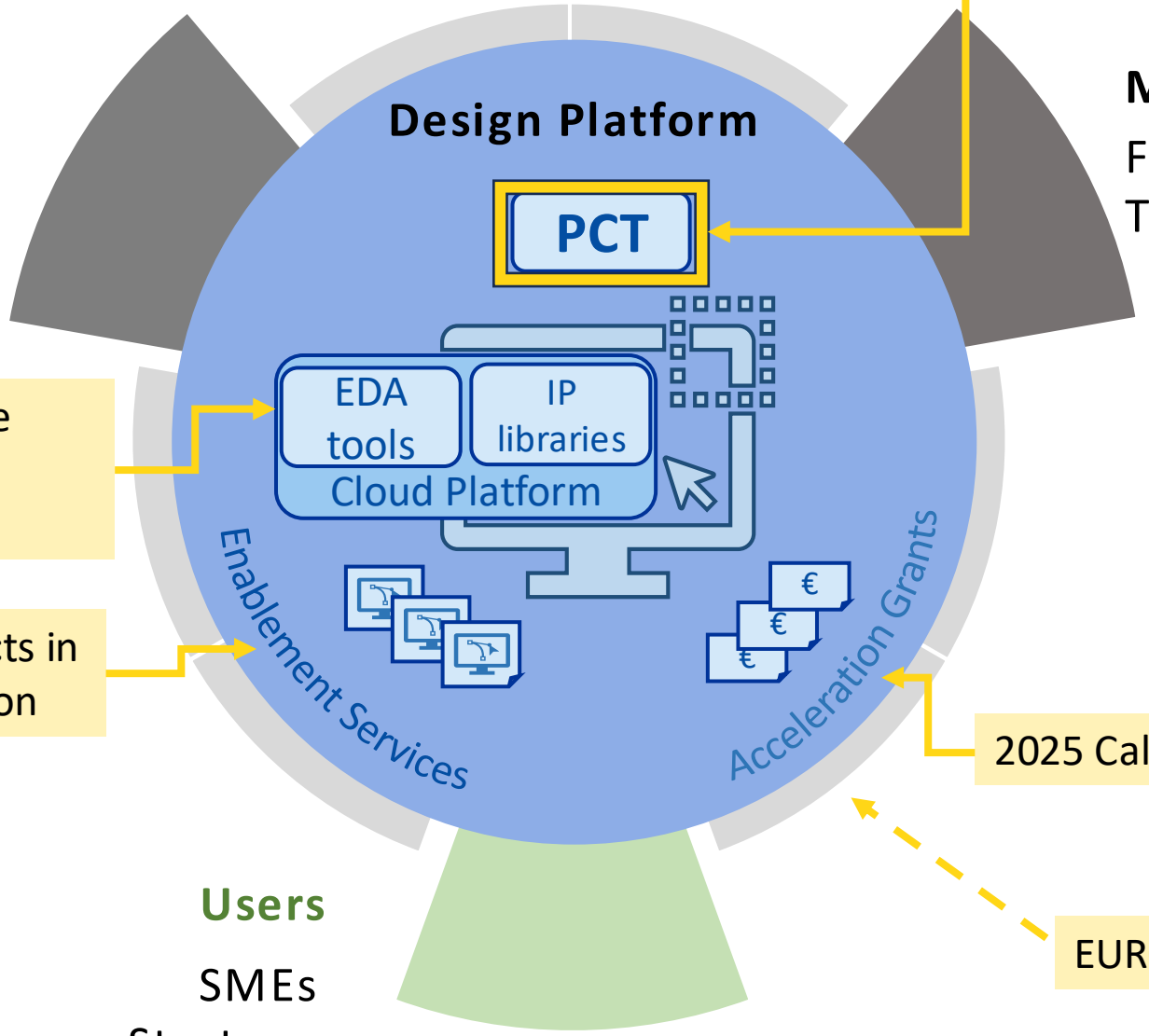
2024 Call for PCT: DECIDE project

Suppliers

EDA, Tools, Services

Manufacturers

Fabs, Packaging, Testing



2025 Call for open source EDA: 3 projects in grant agreement preparation

2025 Call for DETs: 9 projects in grant agreement preparation

2025 Call for support for SMEs

EUROPRACTICE 2.0

Users

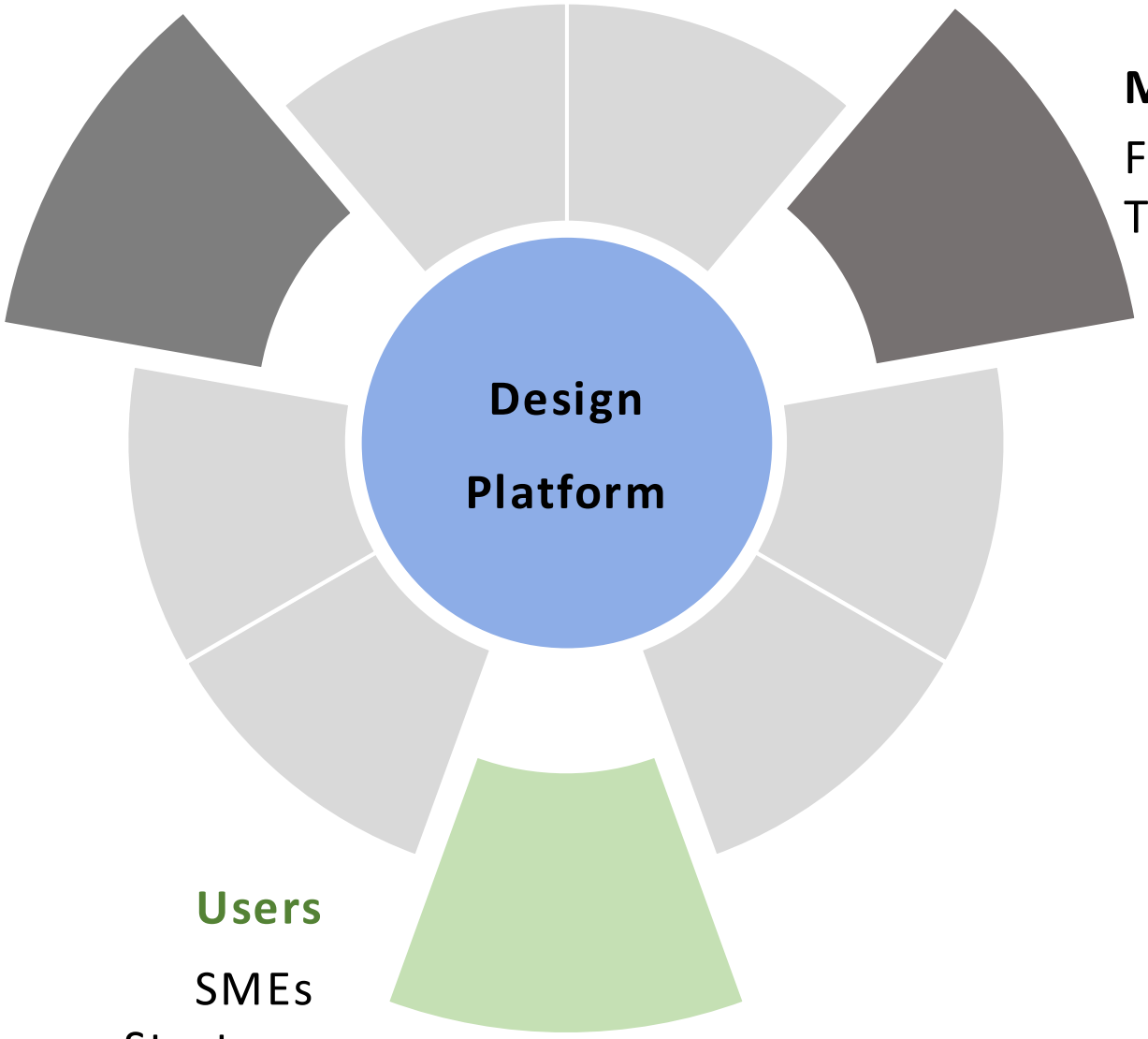
SMEs

Startups

Design Platform

Suppliers

EDA, Tools, Services



Manufacturers

Fabs, Packaging, Testing

Users

SMEs
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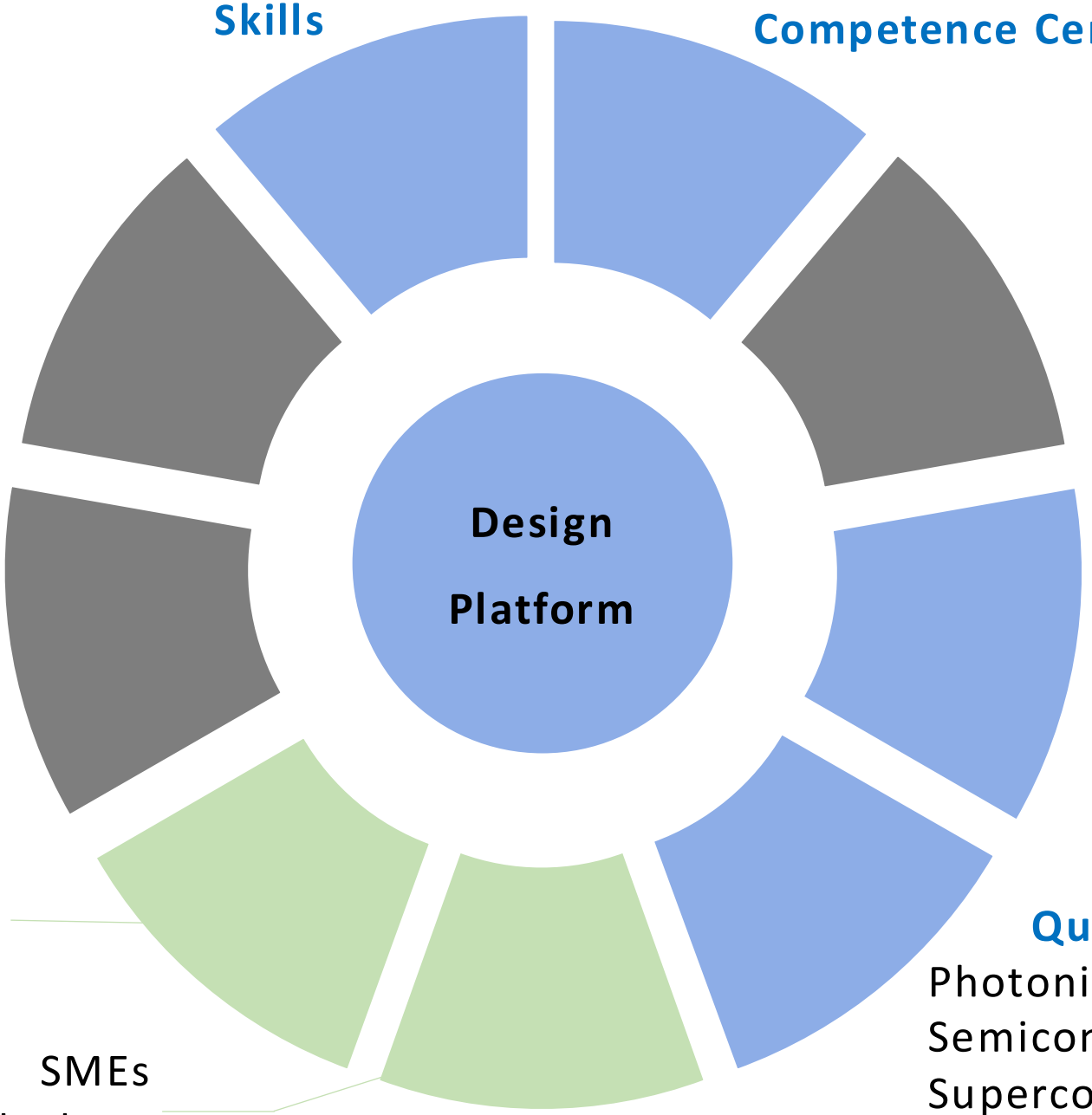
Chips for Europe Initiative



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EUROPEAN PARTNERSHIP

Overview & Governance

A Hub to Support European Chip Design

The Implementation Framework

- **Platform Coordination Team (PCT):** Manages supplier agreements (EDA/IP), coordinates the central cloud, and sets the legal/operational framework.
- **Design Enablement Teams (DETs):** Manage distributed cloud instances and provide hands-on application engineering support.
- **Collaborative Technical Design:** Together, the PCT and DETs design the overarching technical implementation and interfaces for distributed services.

Core Objectives

- **Lower barriers** for IC design, particularly for advanced technologies.
- **Foster collaboration** among EU stakeholders and leverage existing initiatives.
- **Develop skills** via training and support through a network of competence centres.
- **Integrated access** to pilot lines and fabs for early prototyping.
- **Cloud-based infrastructure** providing easy access to tools, kits, flows, and IP libraries.

Supporting Startups and SMEs

Reducing Risk and Accelerating Success

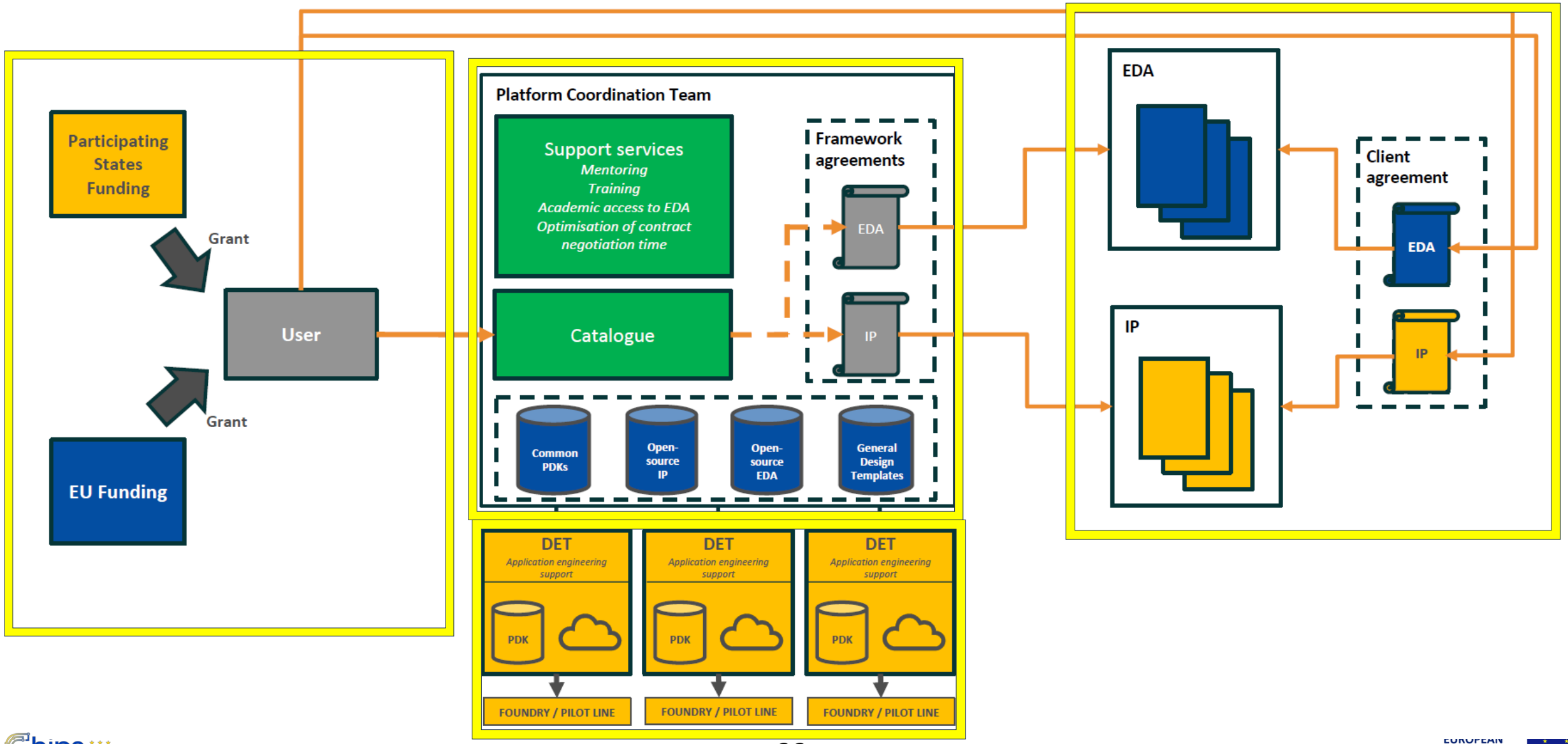
Addressing Critical Needs

- **Access:** A “One-Stop-Shop” for proprietary design tools, **open-source EDA alternatives**, IP, and advanced technologies.
- **Simplicity:** Easy installation and maintenance of design flows, including those from multiple vendors.
- **Talent:** Direct access to people with the right skills and training.
- **Finance:** Facilitating easier access to capital.

The Value Proposition

- **Lower the risk** of entry for new players.
- **Lower time-to-market** for innovative chip designs.
- **Maximize the success rate** of European SMEs in the global market.

Conceptual Architecture of the Design Platform



Expanding the Ecosystem with Open-Source

The Design Platform shall include open-source assets to reduce costs and dependency on proprietary systems

- **Lowering Barriers:** Establish low-barrier access for startups and SMEs through a user-centric service framework.
- **Tool & IP Selection:** Select and integrate **high-quality open-source EDA tools** and services to lower the cost entry barrier.
- **The RISC-V Ecosystem:** Focus on an **open-source IP repository** with a strong presence of RISC-V and the specific EDA tools that support them.
- **Sandbox Environments:** Oversee requirements for procuring and integrating open-source "sandbox" environments for design experimentation.

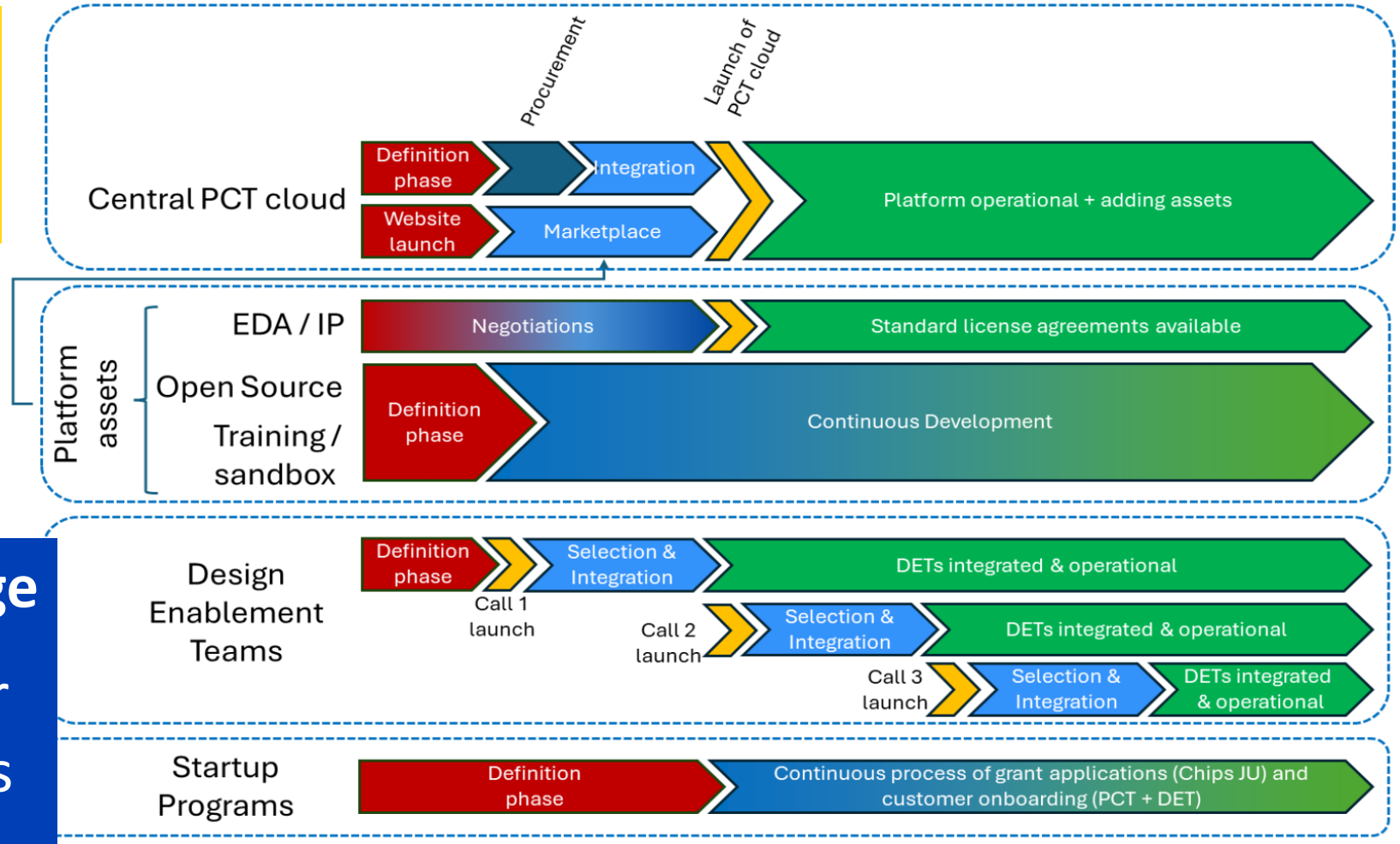
Path to Industry-Grade Silicon

Commercial Coexistence: commercial EDA is currently the primary option for industry-grade chips, but there is place for open-source tools.

Following the initial definition phase, open-source assets move into a state of **continuous development.**

The Industry-grade Challenge

Can open-source EDA deliver industry-grade chips towards the end of this roadmap?



The different phases of the DECIDE implementation plan

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Technical Maturity & Scalability

Challenges	**1.** Can open-source realistically **compete with proprietary** tools on Power, Performance, and Area?
	2. EDA problems are largely NP-hard; matching the **massive algorithmic and compute investment** of commercial giants may be an obstacle for the research community.
	3. Universities often solve specific toolchain fragments. Does the community have the **incentive to build a complete, end-to-end toolchain**?
Opportunities	**1. Hybrid Flows:** Using open-source for rapid prototyping or specific blocks while relying on commercial tools for final sign-off.
	2. AI-Driven Optimization: Leveraging AI/ML to leapfrog traditional optimization bottlenecks.
	3. Architectural modularity and standardized interfaces across the design flow—from system to packaging—to allow new features to integrate seamlessly.

IP, Legal & Reliability

Challenges	**4.** Foundries are traditionally protective of **accessibility to their PDKs**. We need business models that make sharing attractive to them.
	5. Can open-source tools provide the rigorous **Safety-Critical Quality Assurance** required for automotive, medical, or aerospace applications?
Opportunities	**4.** Chips for Europe Initiative **Pilot Lines** are actively working to make PDKs more accessible for European designers.
	5a. The "Red Hat" model, in which a professional entity to offer certified, supported, and holistic open-source toolchains.
	5b. Using the **Design Platform** to provide professional-grade support for open-source flows, as an alternative path to subsidising license fees of SMEs.

Economics & Ecosystem Adoption

Challenges	**6.** What is the **incentive** for a major player to contribute back to the community instead of keeping proprietary advantages?
	7. The Skills gap: Most of the current workforce is trained exclusively on commercial tools.
	8. University-led innovation that turns into a **startup** is often subsequently **acquired** by a commercial vendor.
Opportunities	**6. Shared maintenance:** Promoting business-friendly licenses that allow shared core maintenance while keeping specific competitive features closed.
	7. Silicon-validated PoCs: Reducing the cost of actual tape-outs for training and Proof-of-Concept, moving beyond simulation-only design.
	8. Service-based models: Shifting the value from software sales to customization, specialized design support, and niche optimization.

Expectations – what next?

Near-Term Focus: Rigorous standardization of workflows and interfaces and deep integration of AI/ML

Maintain a tight feedback loop with SMEs to ensure the platform meets real-world business needs.

Explore collaboration in emerging areas like Quantum technologies where the field is still level.

Maximize the networking possibilities of the Chips JU initiatives; the Design Platform, Competence Centres, and Pilot Lines.

Balance research and innovation with a clear focus on High TRLs — getting as close to market as possible.

Thank You

www.chips-ju.europa.eu

Chips_JU

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