

EuroCDP
EU Chips Design
Platform

Open-Source Approach to Lowering Barriers in (P)IC Manufacturing within EuroCDP

David Martín-Sánchez
Eros Camacho

Microelectronics Institute of Sevilla (CSIC)

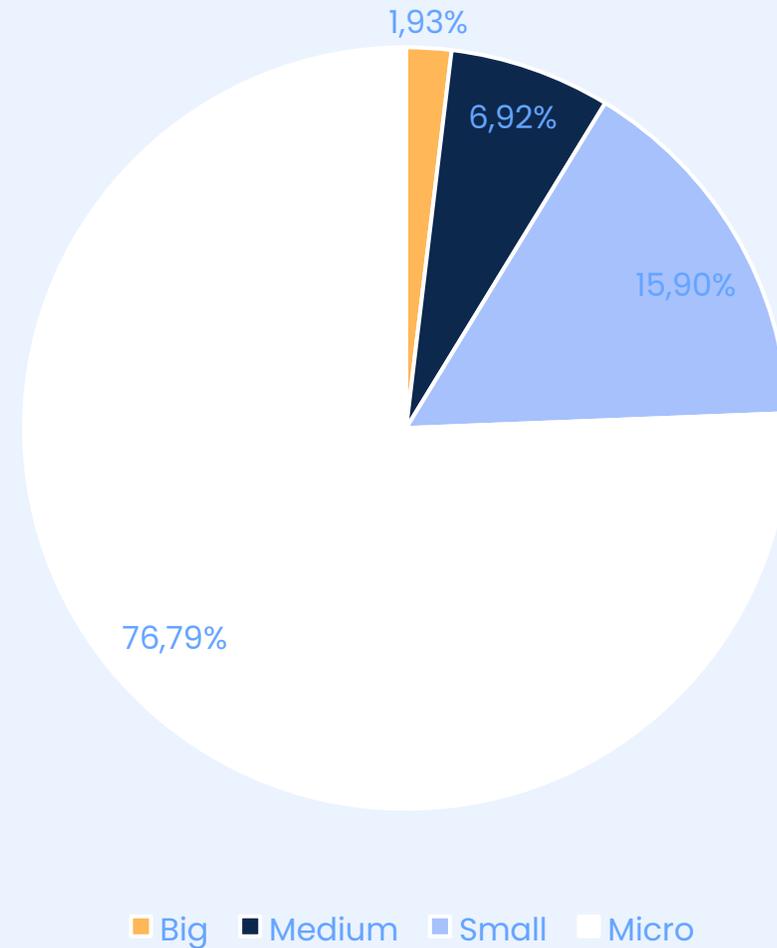
Semiconductor Landscape

- Europe's semiconductor market is **highly concentrated**, led by 4 major companies (ASML, ST, Infineon, NXP) controlling **~65%** of total market value.
- **2** publicly listed fabless in Europe In 2021 (Dialog Semiconductor in UK and Nordic Semiconductor in Norway).
- Design represents **~ 50%** of the market of the semiconductor value chain.
- Fabless **SMEs are essential** for EU resilience and innovation.
- Fabless SMEs face **high entry/scaling barriers** (EDA, IP, Tape out, skill shortage) and **limited funding** (scarce patient capital, fragmented funding)
 - EDA and IP represent between 35% and 45% of the total design cost
- **2 death valleys** to overcome: from **Lab to Prototype** and from **Prototype to Scale**

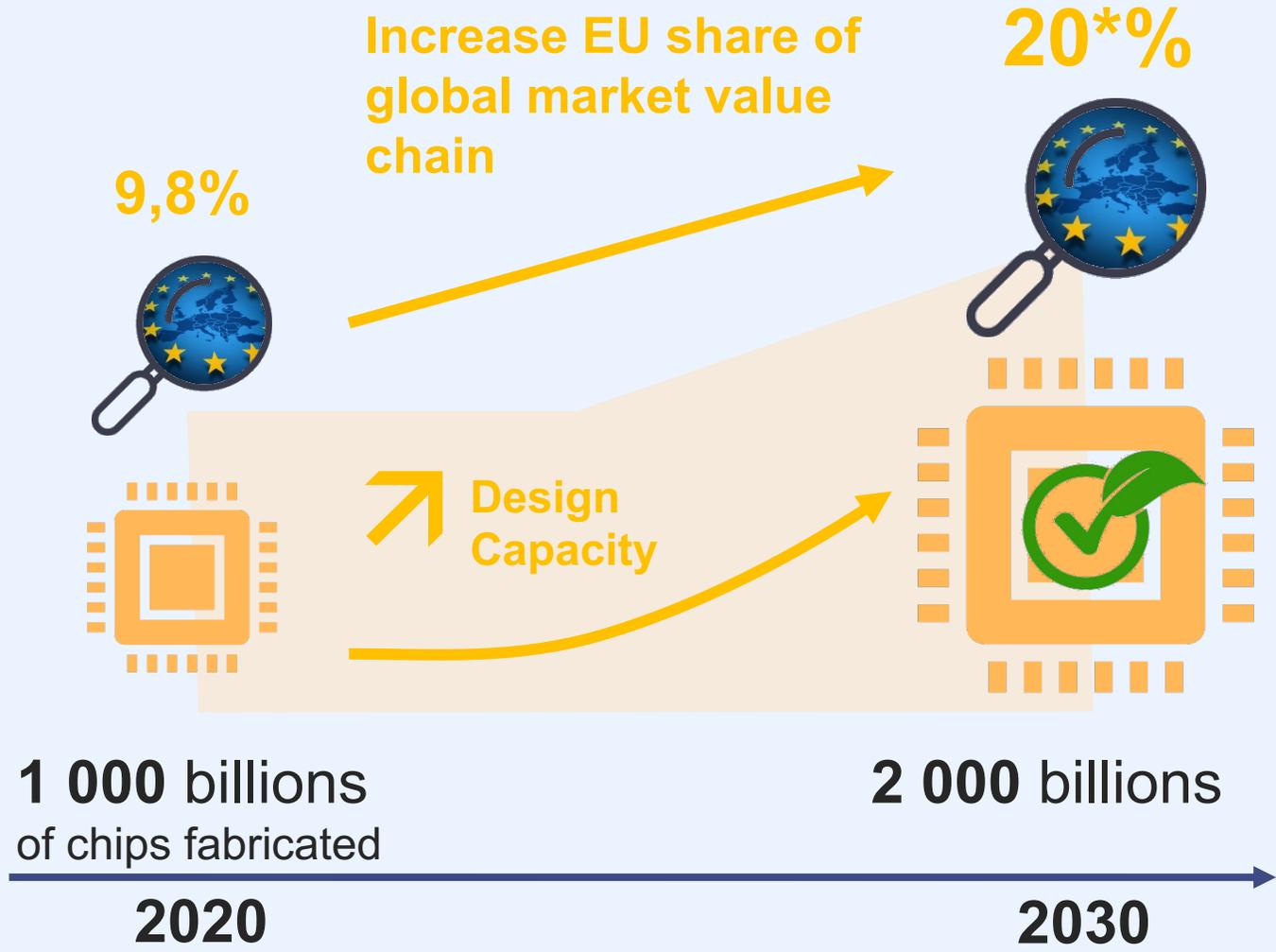
Enterprises by Size in Semiconductor Manufacturing in the EU

~30% of global IC startups are hosted in Europe

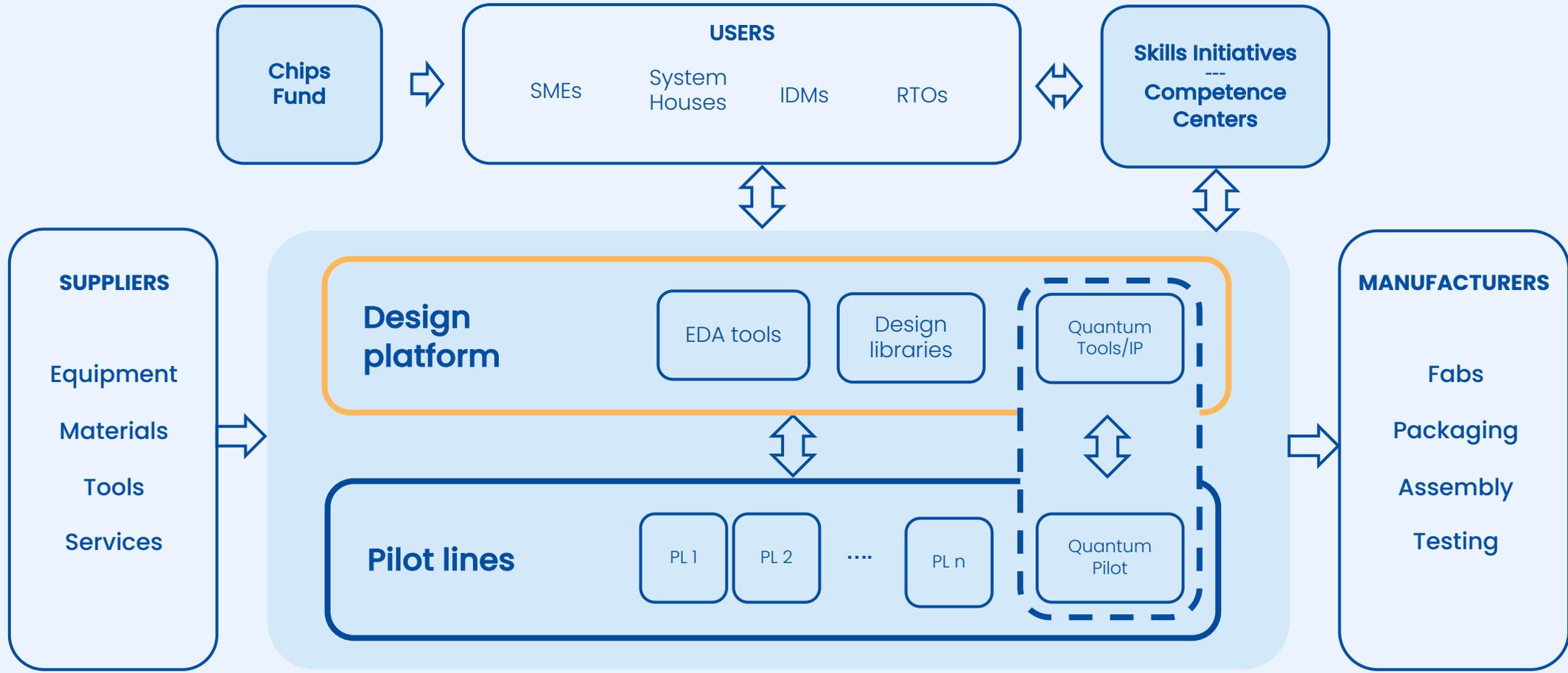
But they attract **only ~6% of global startup funding.**



Chips Act: Make Europe more Digital and Greener

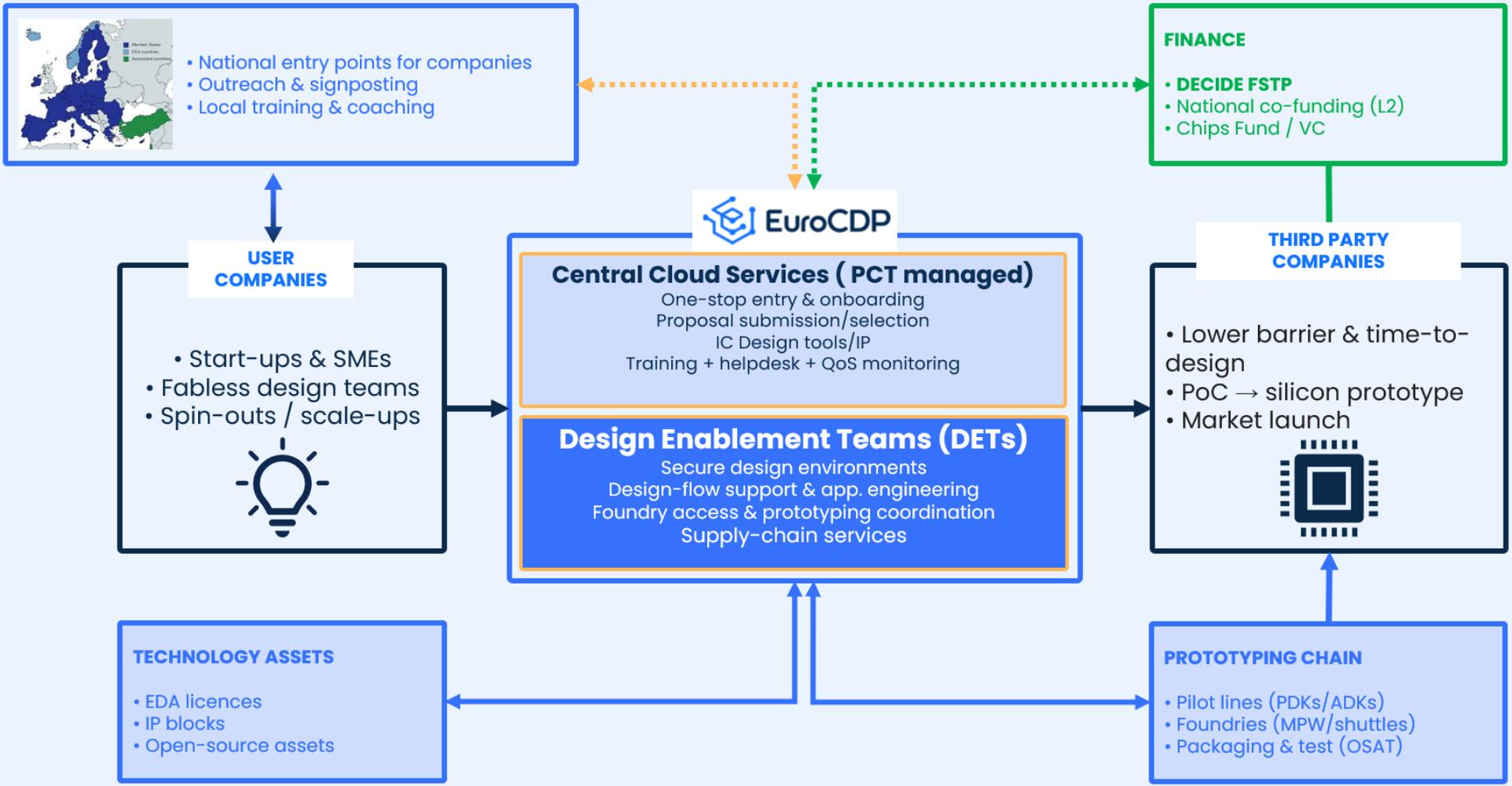


EuroCDP at the heart of EC strategy to reinforce EU Chip market share



EuroCDP at a glance

▶ Reinforce EU design capacities to increase EU fabless market share



EuroCDP PCT Team

► Define, Specify, Administrate & Operate EuroCDP

- 12 partners
- 11 Member States
- 8 RTOs, 4 Universities
- Links to National Chip Competence Centers
- 5 pilot lines representatives
- Europractice representatives
- IC, PIC, Quantum, Open source
- 81 support letters

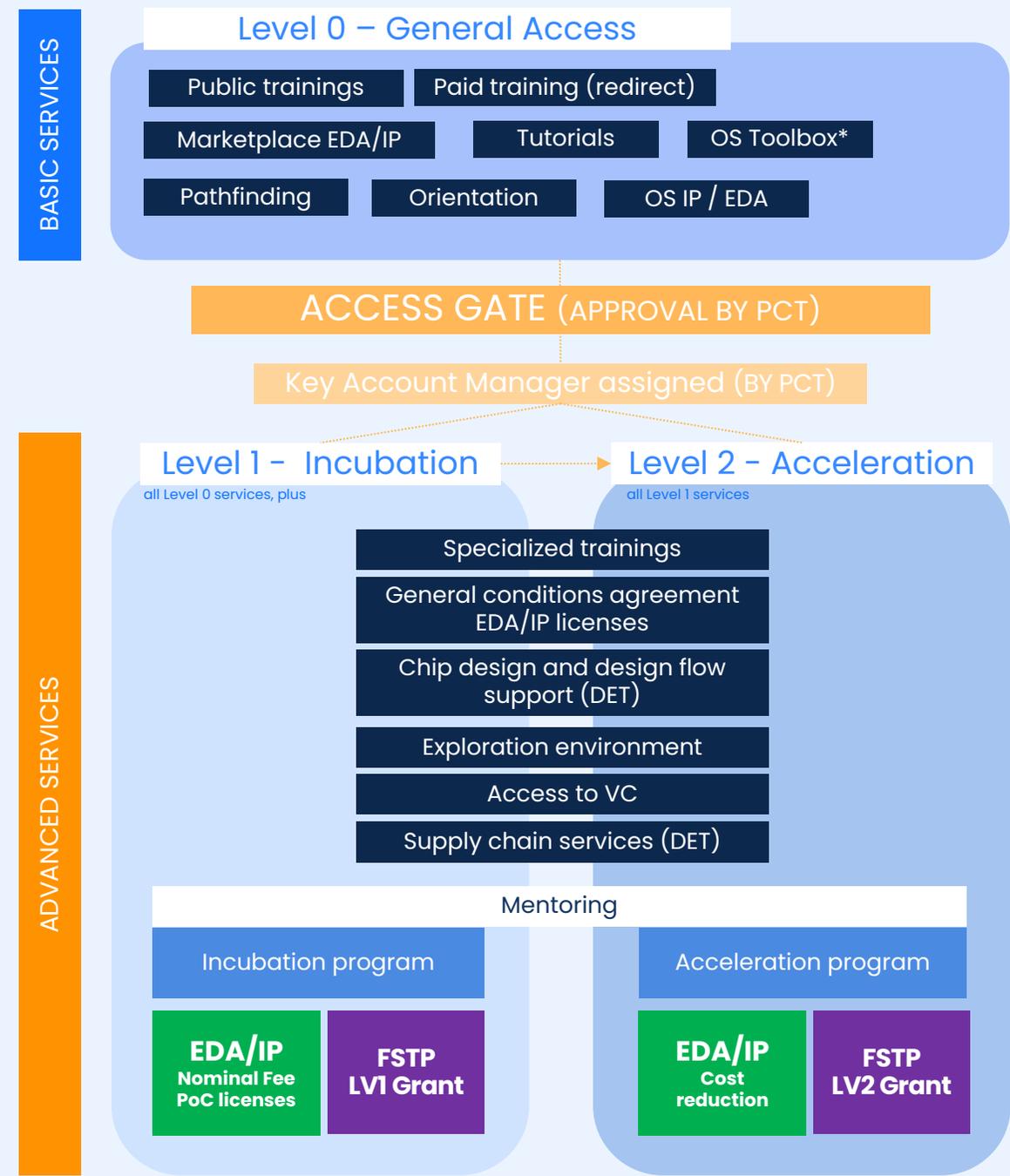


FSTP-DECIDE → EuroCDP advance services

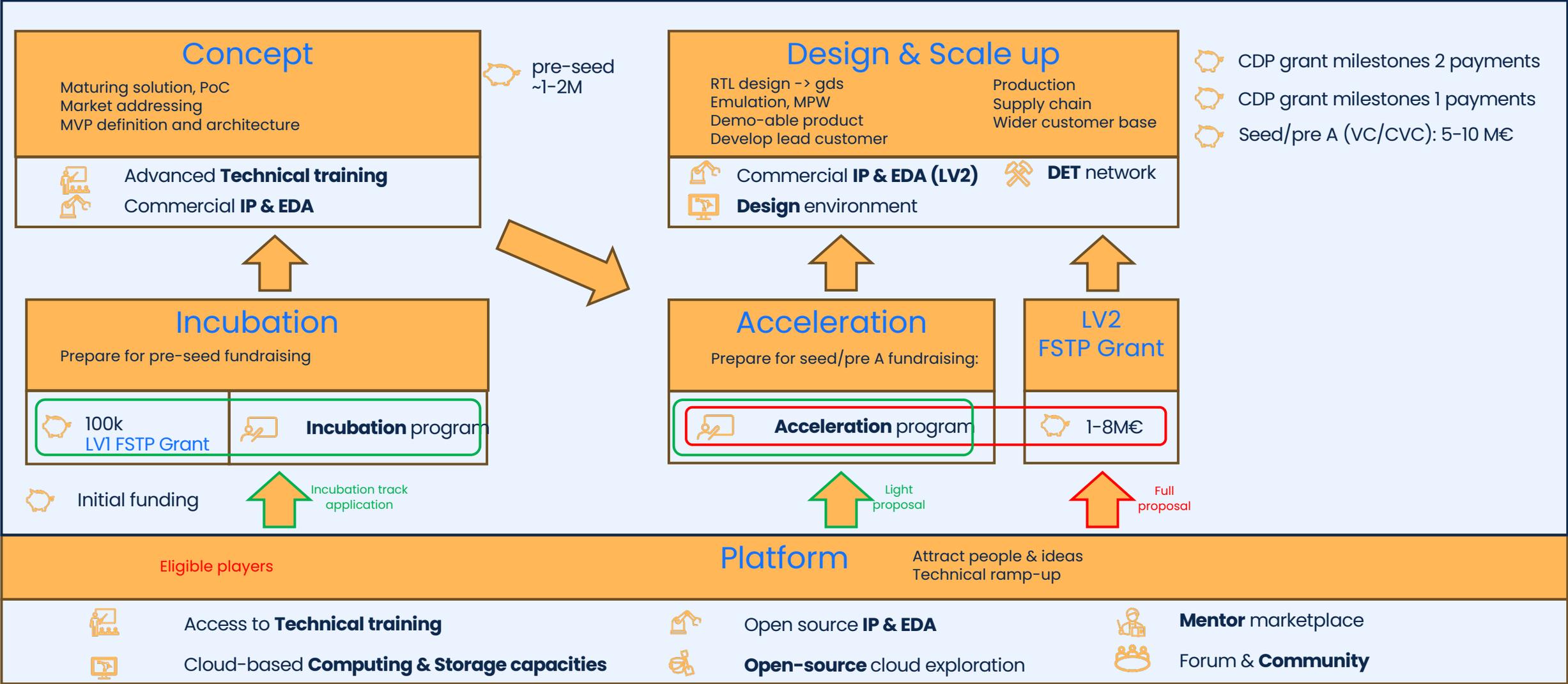


- FSTP-DECIDE allocates **EUR 220 million** in EU funding for this action Both Level 1 and Level 2 companies will benefit from FSTP

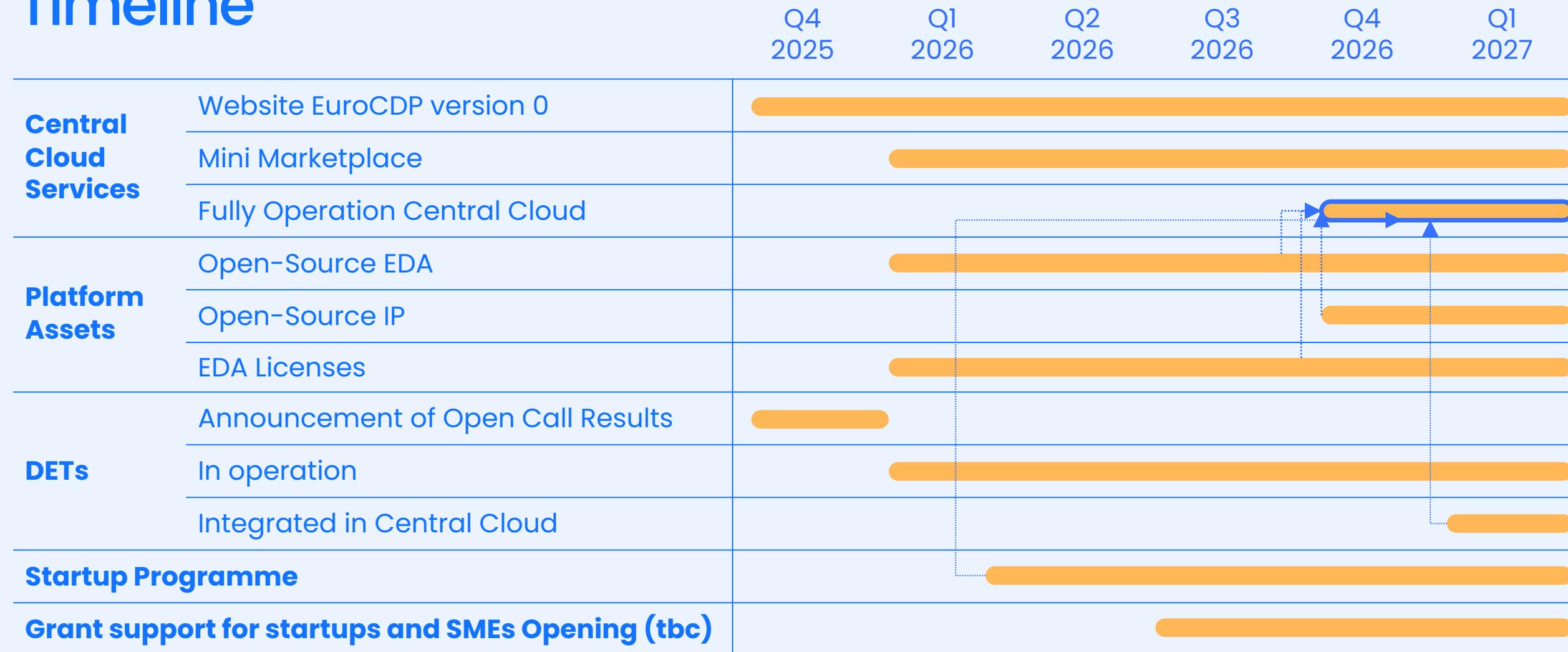
LV1 FSTP Grant	LV2 FSTP Grant
<ul style="list-style-type: none"> ✓ Electronic Design Automation (EDA) tool license costs ✓ Semiconductor Intellectual Property (IP) 	
<ul style="list-style-type: none"> ✓ Travel, accommodation, and subsistence costs to participate in the incubation program 	<ul style="list-style-type: none"> ✓ Fabrication costs.



EuroCDP Advanced Service Flow



EuroCDP Timeline



EuroCDP Value Proposition for EU Fabless

Chip Design Accelerator

- ✓ Cloud-based **Computing & Storage capacities**
- ✓ **End-to-end** Chip design support & services
- ✓ **Supply chain management** from R&D to final test
- ✓ **Open source**
- ✓ **Sandbox** for exploration
- ✓ **Technical training** access

SME Financial Support

- ✓ Users' project **grants** (procurement, manufacturing & DET services)
- ✓ **Negotiated** Commercial EDA & IP licenses

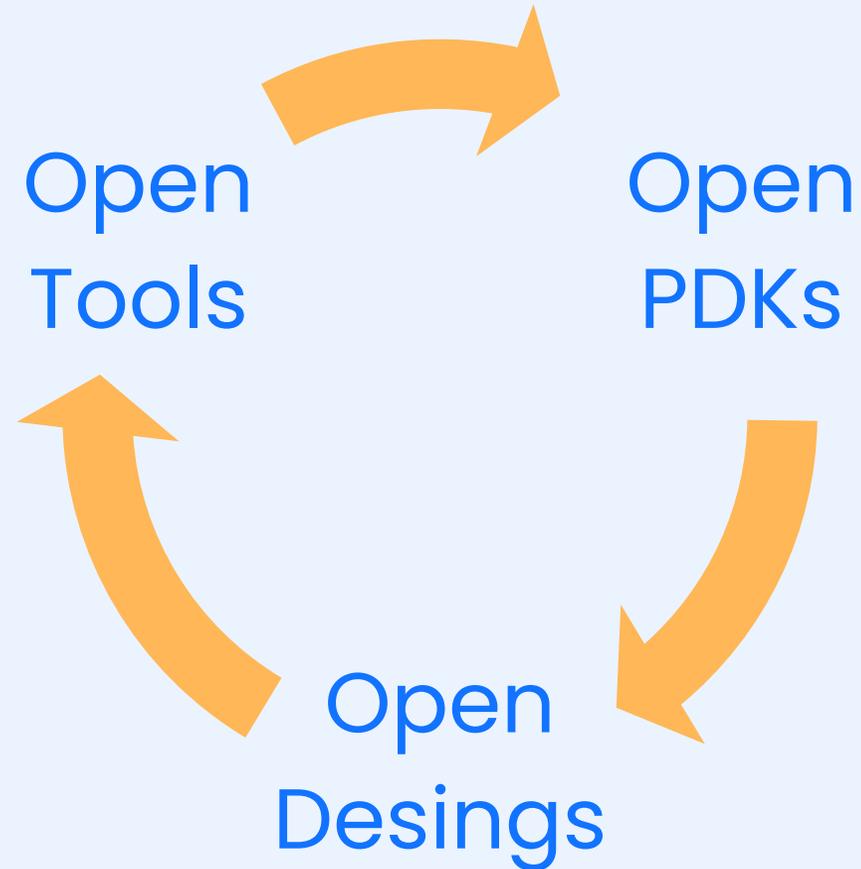
Entrepreneurship Support

- ✓ **Mentoring**
- ✓ **Incubation program** to enable start-ups ideas to take root and grow
- ✓ **Accelerator program** to boost start-ups to scale

EuroCDP: the Open Branch

Five different flows:

- Analog
- RF
- Mixed-Signal
- Digital
- Photonics



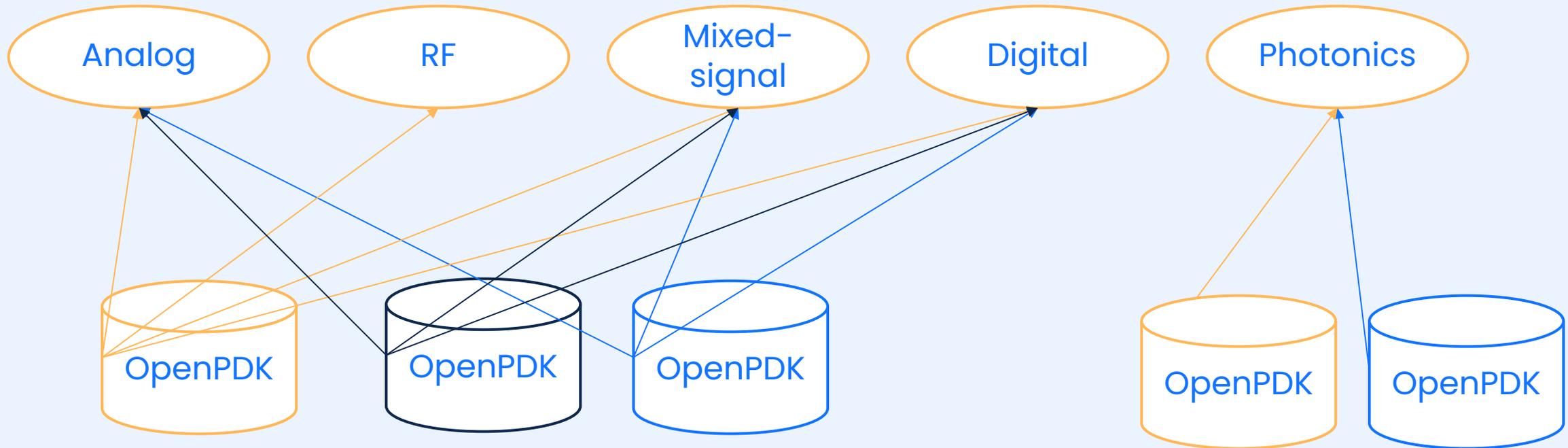
Open source EDA tools



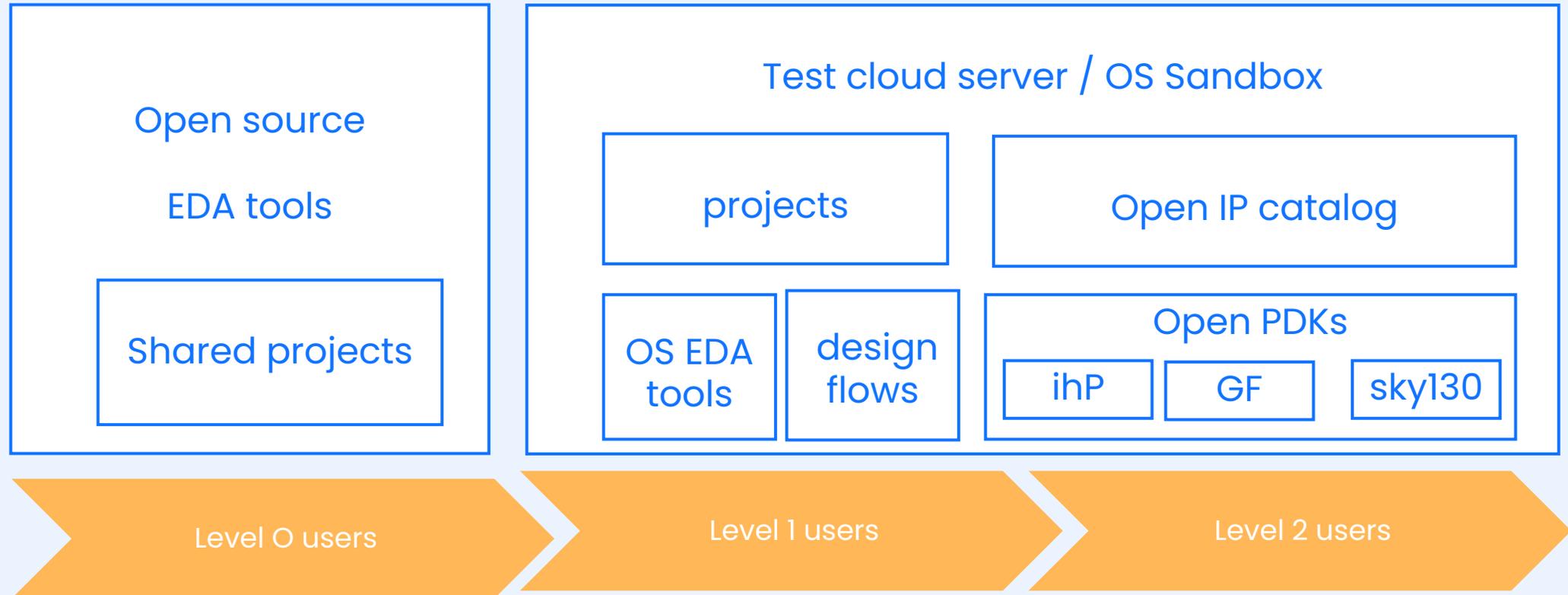
Open IP catalog



Open PDK



EuroCDP journey: The open branch



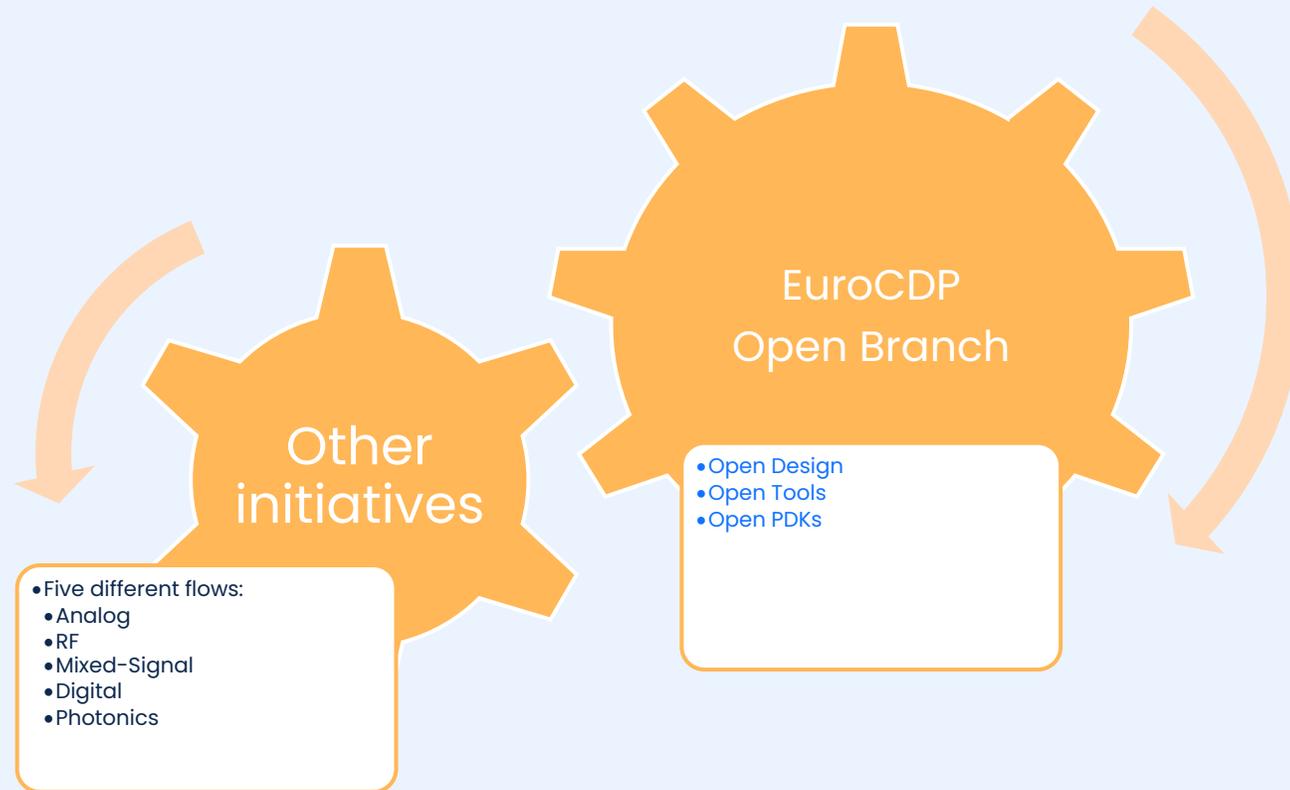
- Training
- Mentoring

- Incubation program

- Acceleration program

FSTP-DECIDE allocates **EUR 220 million** in EU funding for this action
Both Level 1 and Level 2 companies will benefit from FSTP

EuroCDP: the Open Branch



Conclusion

- The EuroCDP doesn't turn his back on Open source users. Open EDA and IP can be complemented with other EuroCDP services.
- Other initiatives will nurture the EuroCDP open branch generating new synergies within the Platform users and services
- The EuroCDP open branch aims to bring OS frameworks to the industry and help make open chips happen.

Feel free to contact us!

From idea to chip — faster, together.

www.eurocdp.eu



EuroCDP

EU Chips Design
Platform