



IHP openPDK and open-silicon MPW: Pushing Open-Source EDA tools to productive digital and analog chip design

HiPEAC 2026

Krakow, Poland, January 28, 2026



IHP at a Glance



Positioning

- ❑ IHP is the **European research and innovation centre for silicon-based systems**, ultrahigh-frequency circuits and technologies
- ❑ **Unique selling point** of a **200mm pilot line** for state-of-the-art BiCMOS technologies, operated under **industry-like conditions, 24/7**, for the provision of prototypes and low-volume production runs.
- ❑ **Qualified technological platform** with direct access for science and industry
- ❑ We offer **130nm CMOS** with additional Bipolar HBT devices for very high frequencies



Vision

"We create foundations and prototype applications based on future silicon-based technologies and systems for a digitalised and networked world as well as for the sustainable preservation of our natural living conditions."

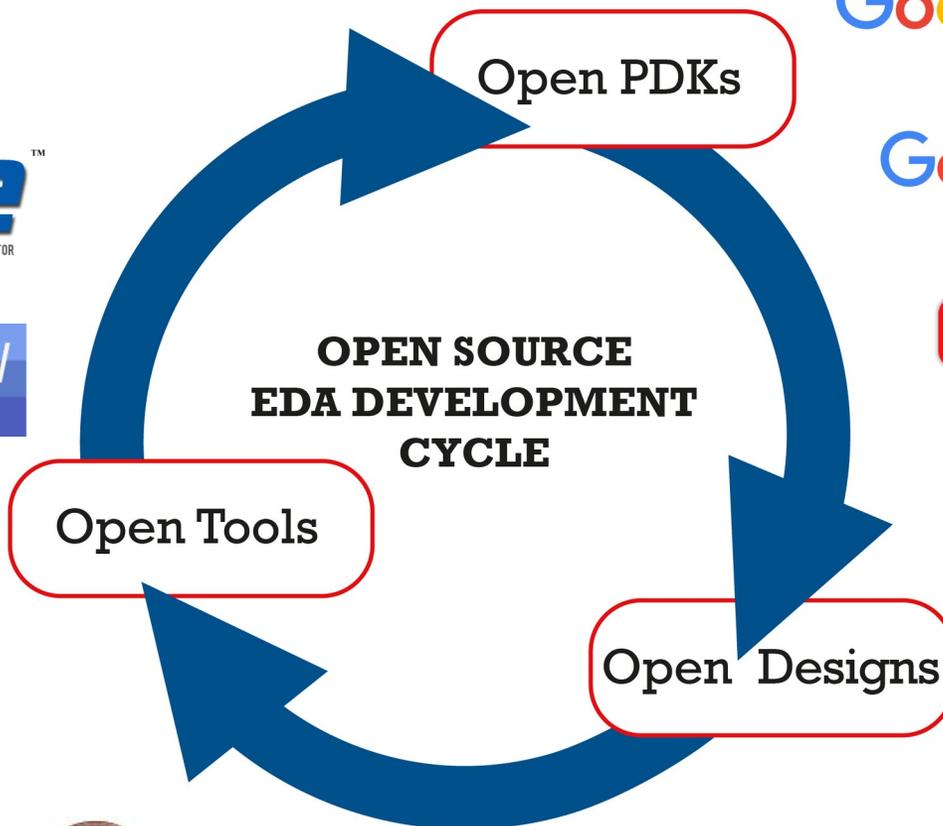
130nm SiGe BiCMOS Technologies for RF Applications



	SG13S	SG13G2	SG13G3Cu
SiGe-HBT f_t/f_{max}	250 / 340 GHz	350 / 450 GHz	470 / 650 GHz
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CEO}	1.7 V	1.6 V	1.5 V
CMOS node	130 nm		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
Resistors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	2.1 fF / μm^2
Metallization	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	*Cu: 4 + 2 (3 μm) Al: 2 (3 μm) *Cu BEOL from X FAB

- Target are **high end developments** for RF & Terahertz frequencies, cryo and space applications
- SG13S & SG13G2 are qualified and ready for **Low Volume of high end products** **SG13G2** technology was selected for the development of an **open PDK**
- SG13G3Cu stable, qualification ongoing

Open Source silicon ecosystem



Google + skywater 130 nm CMOS

Google + GLOBAL FOUNDRIES 500 nm CMOS

IHP-Open-PDK 130 nm BiCMOS

Open PDKs in Japan, China in preparation



Google free open MPW

test cases, regression tests, benchmarks, use cases, user stories, feedback, error reports, feature requests

Motivation for IHP's open Process Design Kit (PDK) initiative



- 0 **Simplify access to education** materials for chip designers and to attract young people to get into chip design process
- 0 Provide **low threshold (cost/technological) access to technology & PDK** for chip designer, academic projects
- 0 **Initiate cooperation's** and joint projects with open source community
- 0 **Be a pioneer** in demonstrating the possibilities of open source EDA software
- 0 To **convince commercial fabs** to support the open source approach

- 0 Support chip design possibilities for **advance IC design projects** by **StartUp, SMEs and commercial companies**

OpenPDK on GitHub



IHP-GmbH / IHP-Open-PDK

Code Issues 181 Pull requests 20 Discussions Actions Projects 1 Wiki Security 7 Insights Settings

IHP-Open-PDK Public

main 3 Branches 2 Tags

Go to file

Code

KrzysztofHerman Merge pull request #762 from IHP-GmbH/dev a2bf8ea · last month 1,310 Commits

File	Commit Message	Time
.github	.github: workflow: drc_regression: Always Pass Test	2 months ago
ihp-sg13g2	updated openems submodule	last month
.flake8	Fixing some linting issues for run_lvs script	2 years ago
.gitignore	Sync with dev branch	5 months ago
.gitmodules	feat(AWS Palace): added gds2palace submodule repos...	2 months ago
.rubocop.yml	KLayout DRC: restructure, cleanup, full min rule set. Q...	8 months ago
AUTHORS	Update AUTHORS file with new contributors	2 months ago
CHANGELOG.md	Update CHANGELOG.md	2 years ago
CODE_OF_CONDUCT.md	Create CODE_OF_CONDUCT.md	3 years ago
CONTRIBUTING.md	added contributing guidelines	3 years ago
LICENSE	Initial commit	4 years ago
Makefile	KLayout DRC: restructure, cleanup, full min rule set. Q...	8 months ago
README.md	Add installation notice to README	last month
requirements.txt	Modify .github/workflows/lvs_regression.yml 4th	4 months ago
versions.txt	versions.txt: Update versions for xschem, qucs-s, klayo...	3 months ago

Readme Apache-2.0 license Code of conduct Contributing Activity Custom properties 665 stars 31 watching 123 forks Audit log Report repository

Releases 2 tags Create a new release

Contributors 35 + 21 contributors

README Code of conduct Contributing Apache-2.0 license

IHP Open Source PDK

IHP-Open-PDK GitHub repository, <https://github.com/IHP-GmbH/IHP-Open-PDK>, accessed: 2026-01-27.

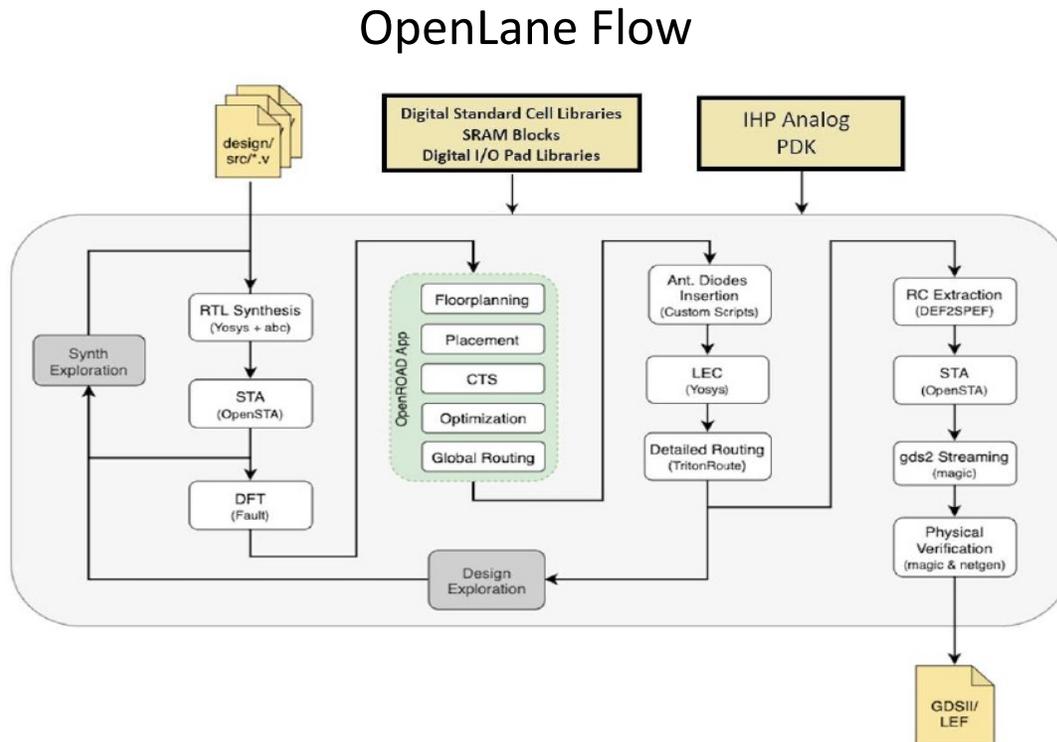
PDK Contents:

- Project Roadmap Gantt chart
- Standard logic cells (Open130-G2)
- SRAM cells, IO cells
- Primitive devices (GDS)
- Klayout tool data:
 - Layer property & tech files
 - DRC deck
 - LVS deck
 - Pycells (+ API)
 - Xsection initial settings
 - 2.5D viewer configuration
- Magic tool data:
 - tech files, parasitic extraction rules
 - DRC rules
 - LVS rules
- ngspice/Xyce simulation models
- xschem:
 - device symbols, settings, testbenches
 - stdcells symbols
- Qucs-S symbols and examples
- OpenEMS/Palace: tutorials, scripts, documentation
- SG13G2 Process Specification & Layout Rules
- MOS/HBT/Passive devices measurement data
- GDS QA Test structures for DRC/LVS

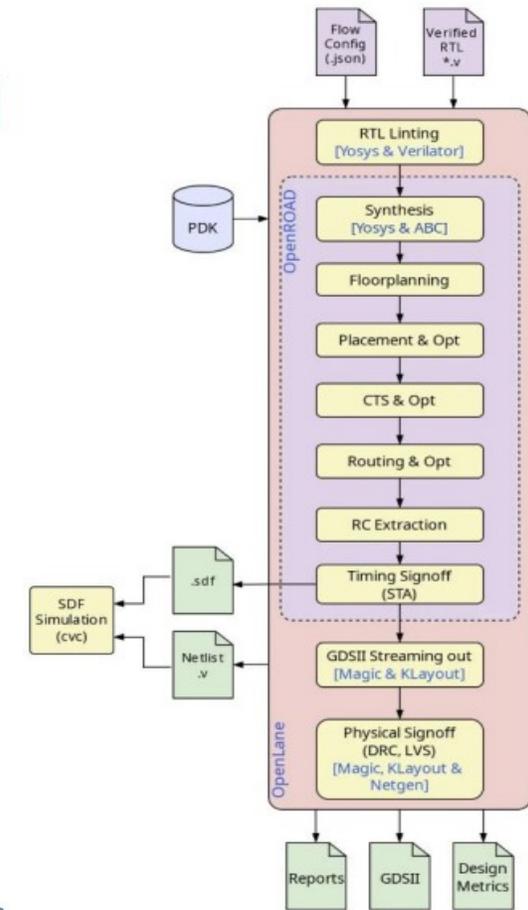
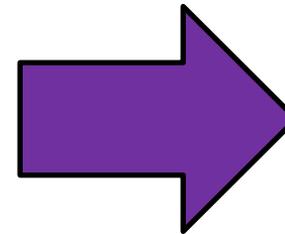
Digital Open Source Design Flow



- 0 Digital Libraries
- 0 Open Road Flow/Apps supported
- 0 <https://github.com/IHP-GmbH/ihp-sg13g2-librelane-template>



LibreLane



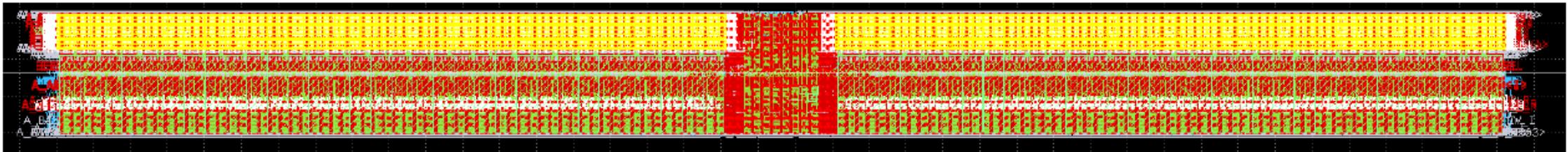
OpenPDK Digital Libraries



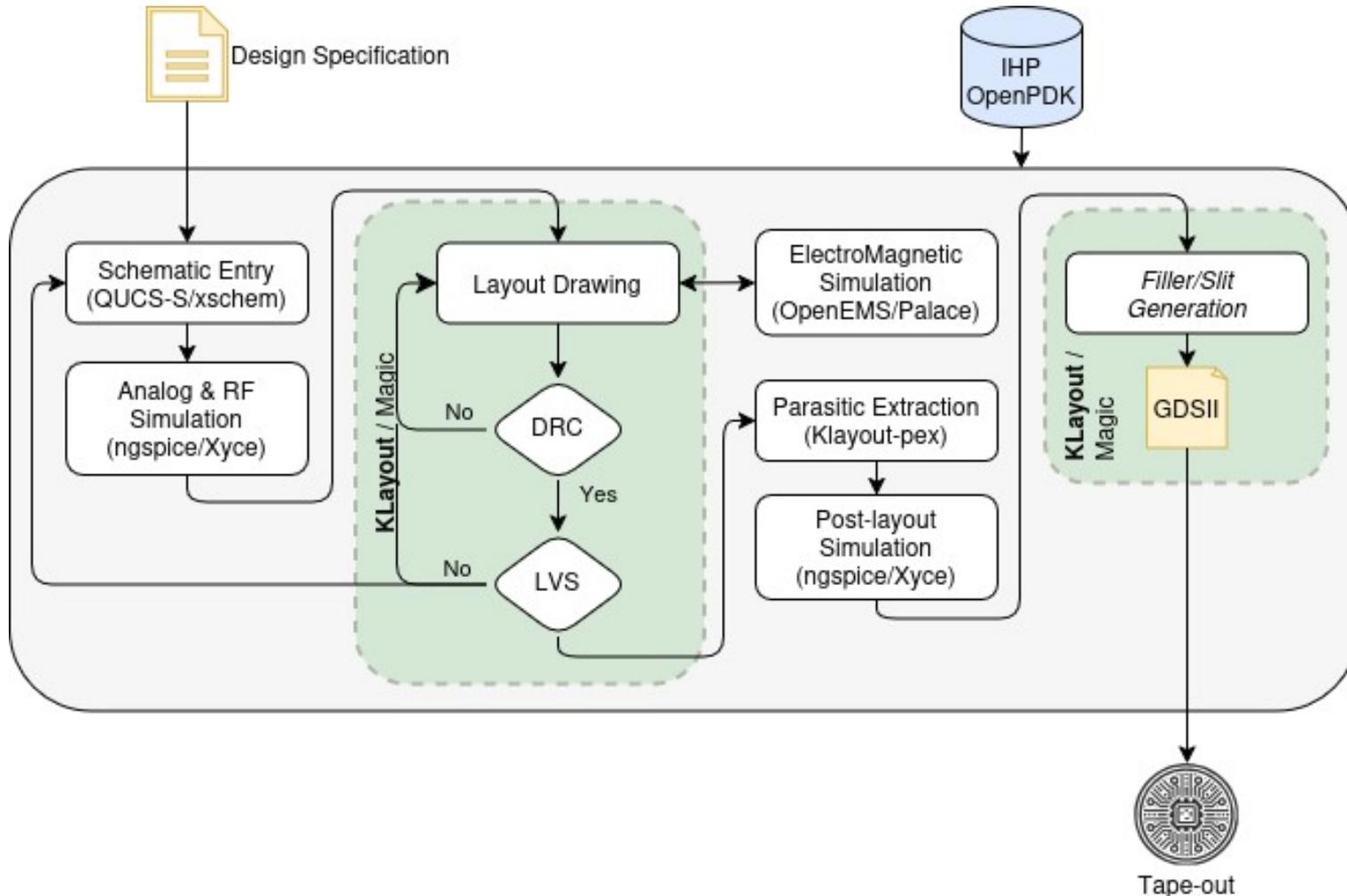
	StdCells	IOCells	SRAM
Verilog	X	X	X
LIB	X	X	X
LEF	X	X	X
CDL	X	X	X
SPICE	X	X	-
GDS	X	X	X

Digital components

- Celllists
 - 84 cells,
 - combinatorial logic,
 - sequential elements,
 - scan flops,
 - clock-gates
- IO- Cells
 - In, Out, InOut, Analog
 - different drive strengths
- SRAM
 - hard macros of SRAM blocks with different sizes
 - SRAM generator in preparation



Analog/RF Open Design Flow



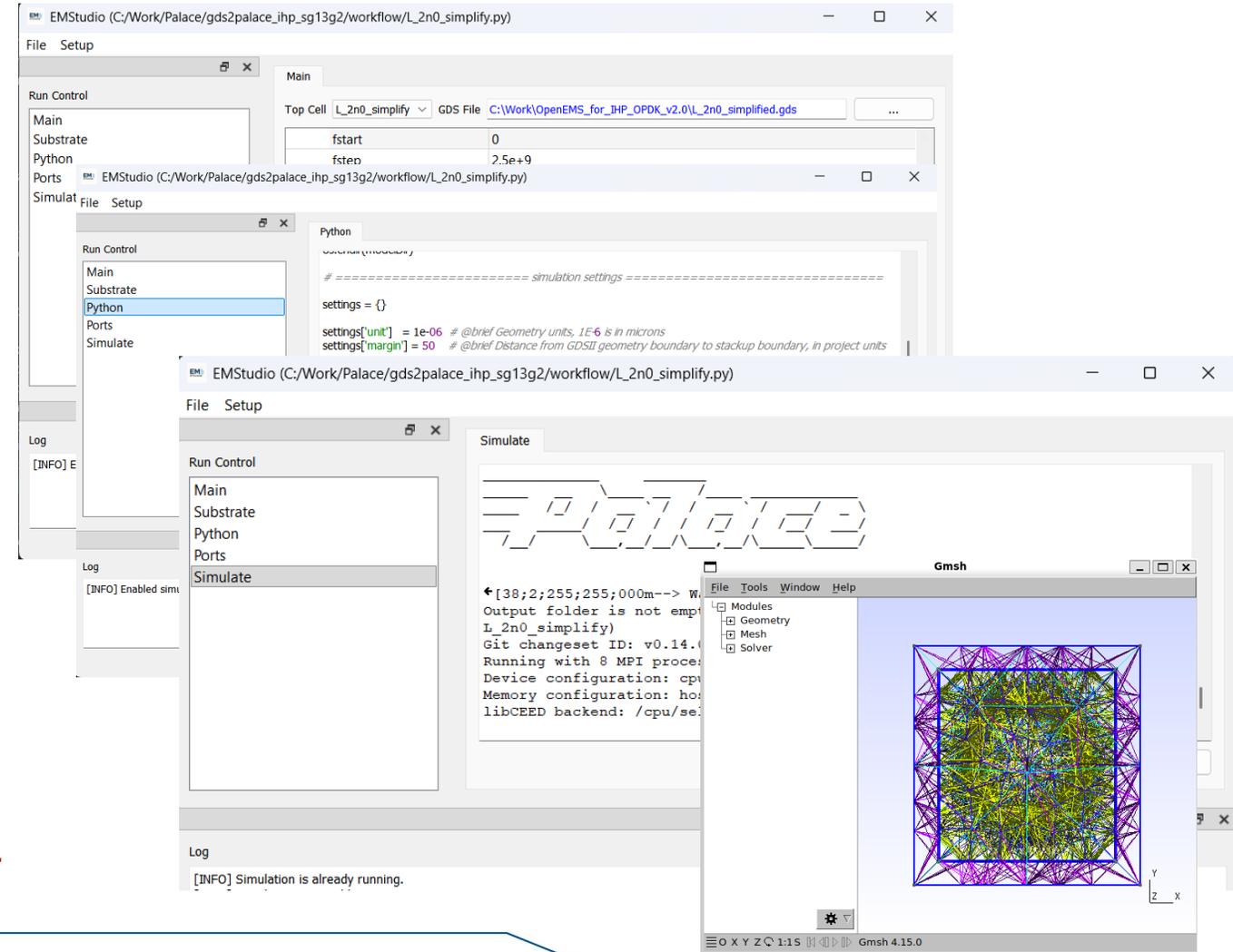
- KLayout-oriented flow
 - Layout design
 - Parameterizable cells
 - Physical Verification
- QUCS-S, xschem
- ngspice, Xyce
- OpenEMS, Palace/AWS (Elmer FEM, under evaluation)
- KLayout-PEX (in development)
- Magic VLSI

EMStudio (One Workflow for multiple EM Solvers)

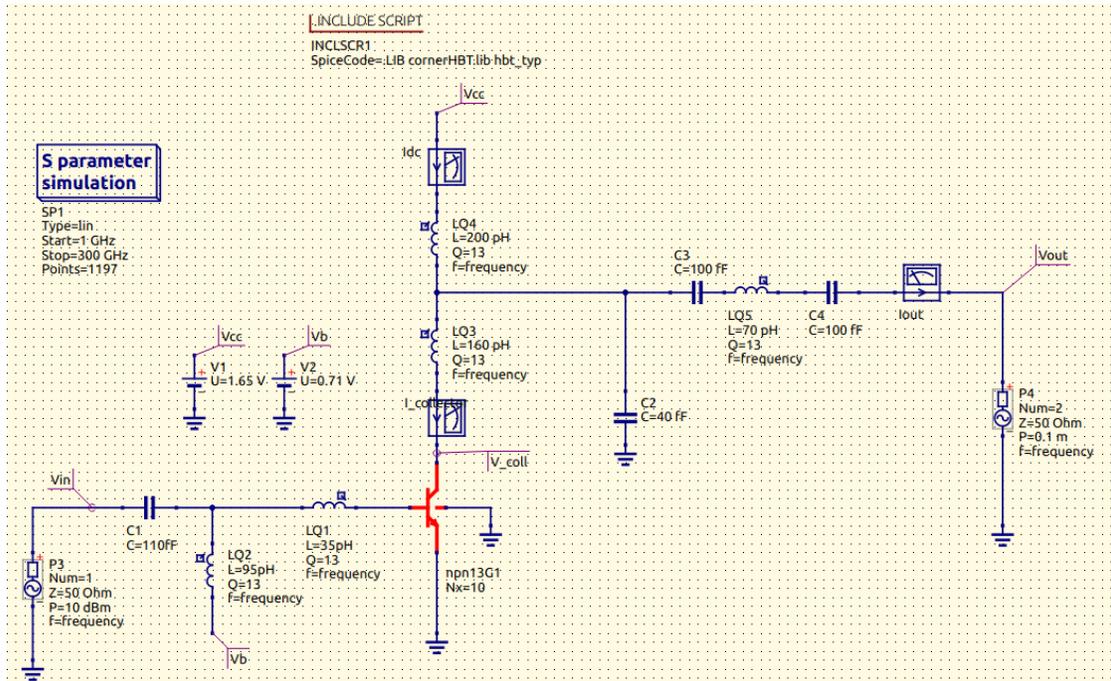


- Setup, execution, and analysis of EM simulations
- Integration with external EM solvers (OpenEMS / PALACE)
- GUI-based tool to simplify complex simulation flows
- Python-based model description
- Cross-platform: Windows (installer provided), Linux (build from source)
- Repository:

<https://github.com/IHP-GmbH/EMStudio>

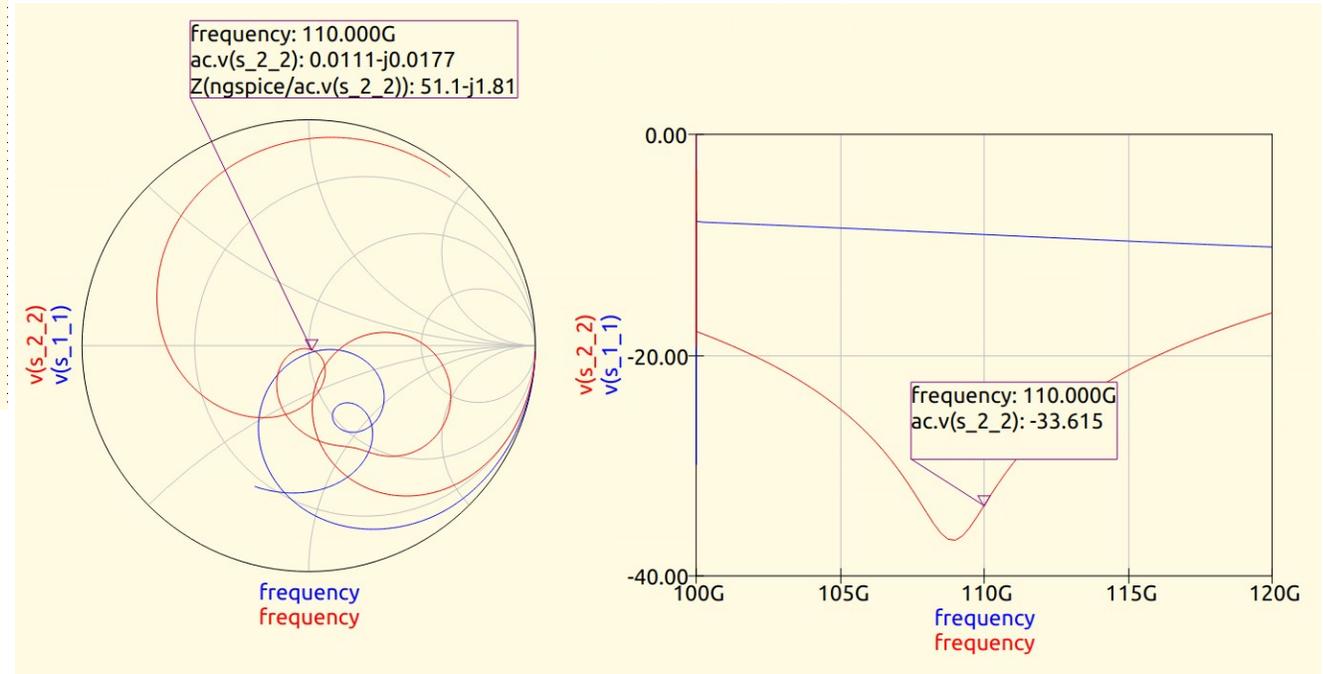


RF design in QUCS-S



- CDL export functionality available (LVS)
- Connection to layout (EM solver) is not there yet
- RF noise simulation features not implemented

S-parameter simulation with Ngspice



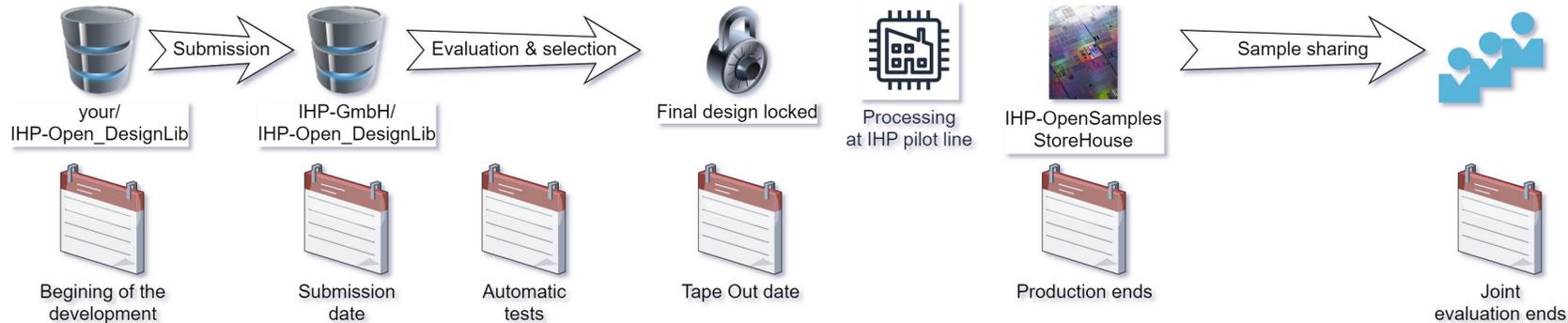
Free MPW Runs - support open source PDK & design



0 The table provides schedule of MPW Runs within FMD-QNC project in 2024 and 2025

Tape out date	22/05/24	11/11/24	22/11/24	07/04/25	09/05/25	18/07/25	15/09/25
Technology	SG13G2	SG13CMOS	SG13G2	SG13G2	SG13G2	SG13G2	SG13CMOS
Area [mm ²]	10	220	20	140	30	30	220

For more details check: <https://ihp-open-ip.readthedocs.io/en/latest/>

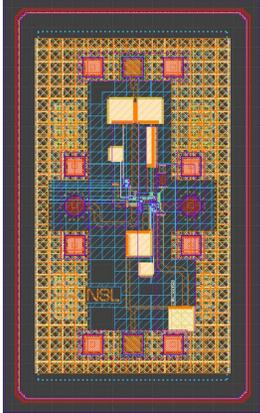


0 Project funds were used exclusively to produce chip designs for non-economic activities, such as university education, research projects, and others

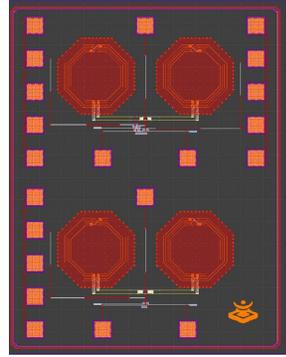
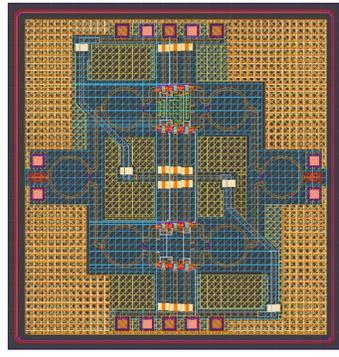
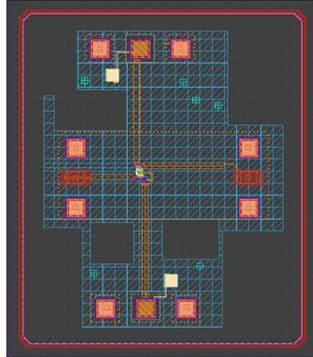
Example - April-2025 – first RF designs, 2 Tiny Tape Out



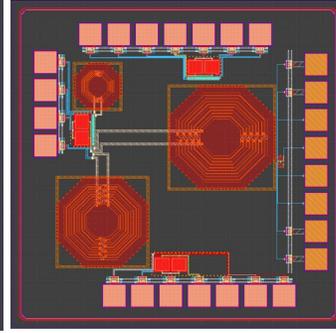
97 GHz TIA



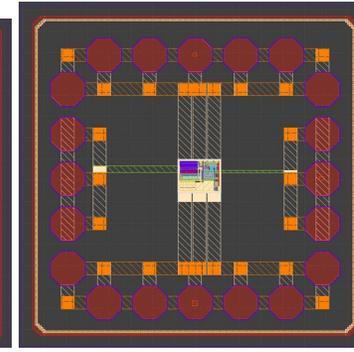
DC to 130 GHz TIA 4-way 180 GHz PA 5GHz Mixer



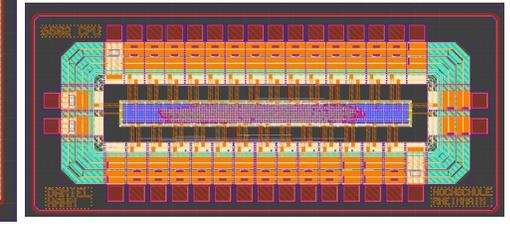
GPS LNA



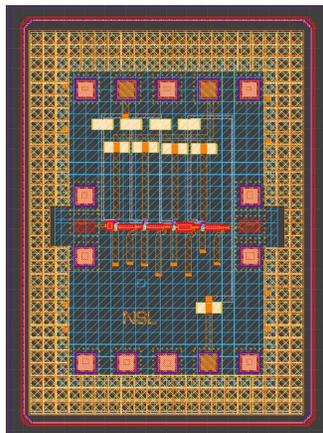
BG - Vref



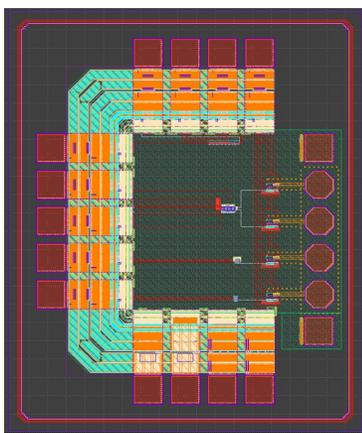
6502 cpu



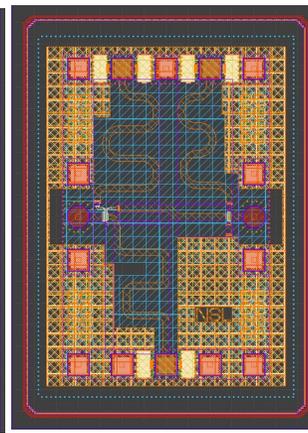
160 GHz LNA



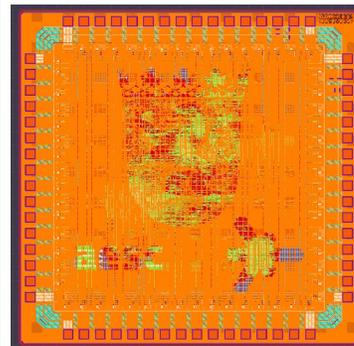
Active L VCO



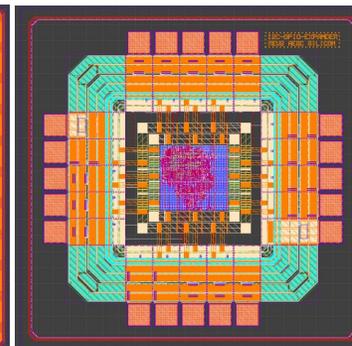
40 GHz LN TIA



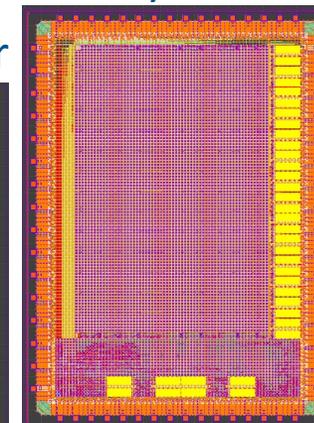
ElemRV-N



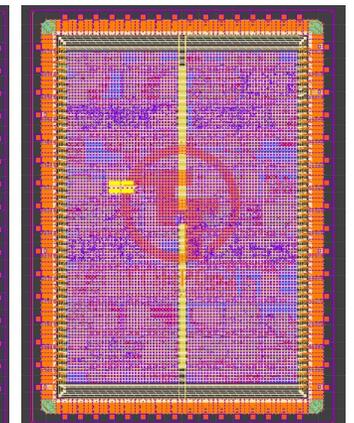
I2c-gpio-expander



Greyhound



2x TT



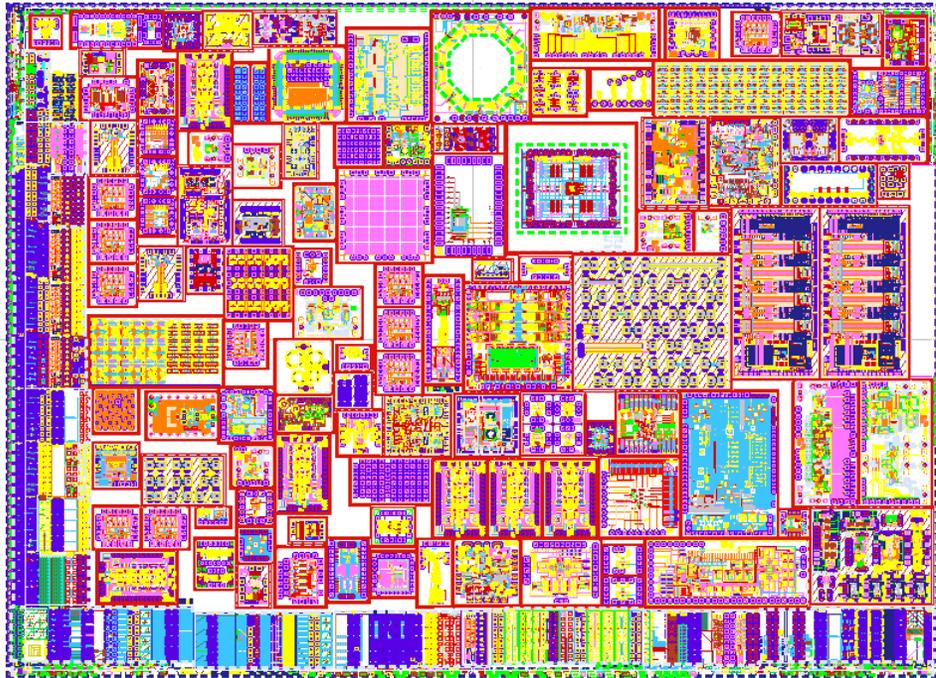
Submission's from open-source community



	Analog	Digital	RF	Mixed	Test structures	Total
May-24	1	2		1	1	5
Nov-24	3	5		1	2	11
Dec-25	5				4	9
Apr-25	1	7	12		2	22
May-25		1	13			14
Sep-25	1	11		3	19	34

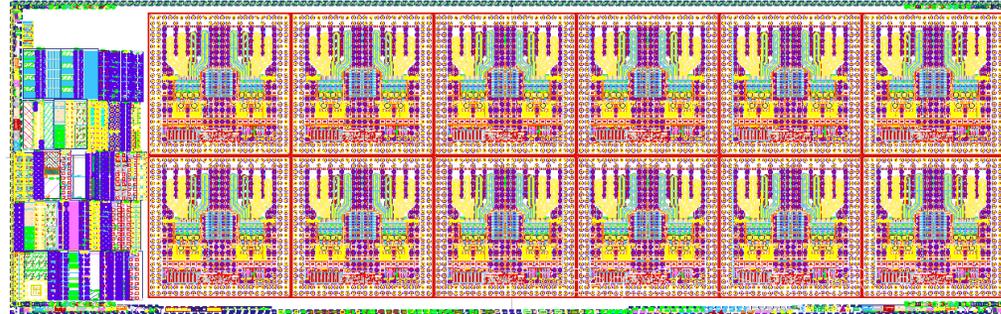
- 0 Many contributions were submitted as a first tape out experience
- 0 All RF designs were the first trailas using open-source approach
- 0 We had contributions from the following countries: Germany, Swiss, Austria, France, Chile, Brasil, USA, Lithuania, Bangladesh, India, Pakistan, Japan, UK
- 0 **95** designs submitted (including 3 time Tiny Tape Outs with **723** desings)

Examples SG13 MPW mask reticles

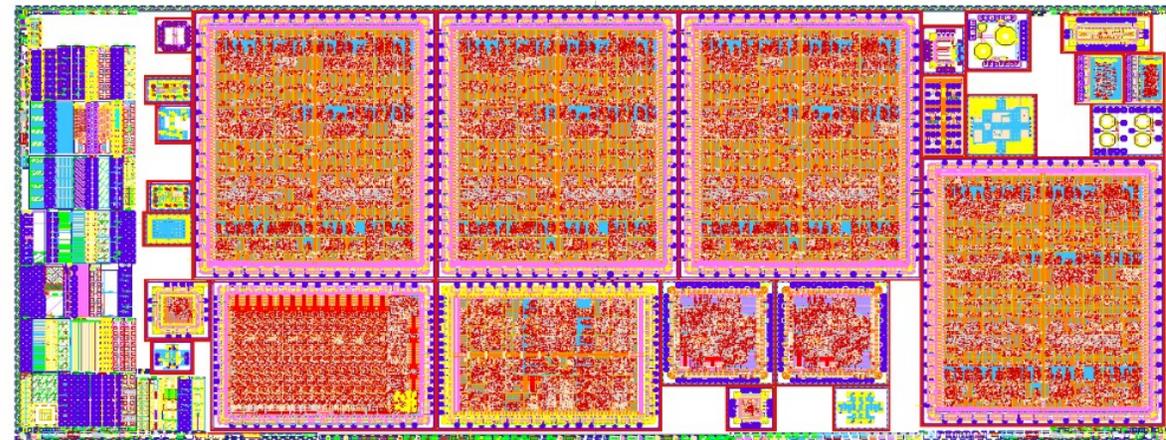


MPW with 113 designs different technologies and modules

IHP MPW **unique selling point** – **maximum flexibility** on design layout dimensions



Product Mask reticle



Open MPW May 2025

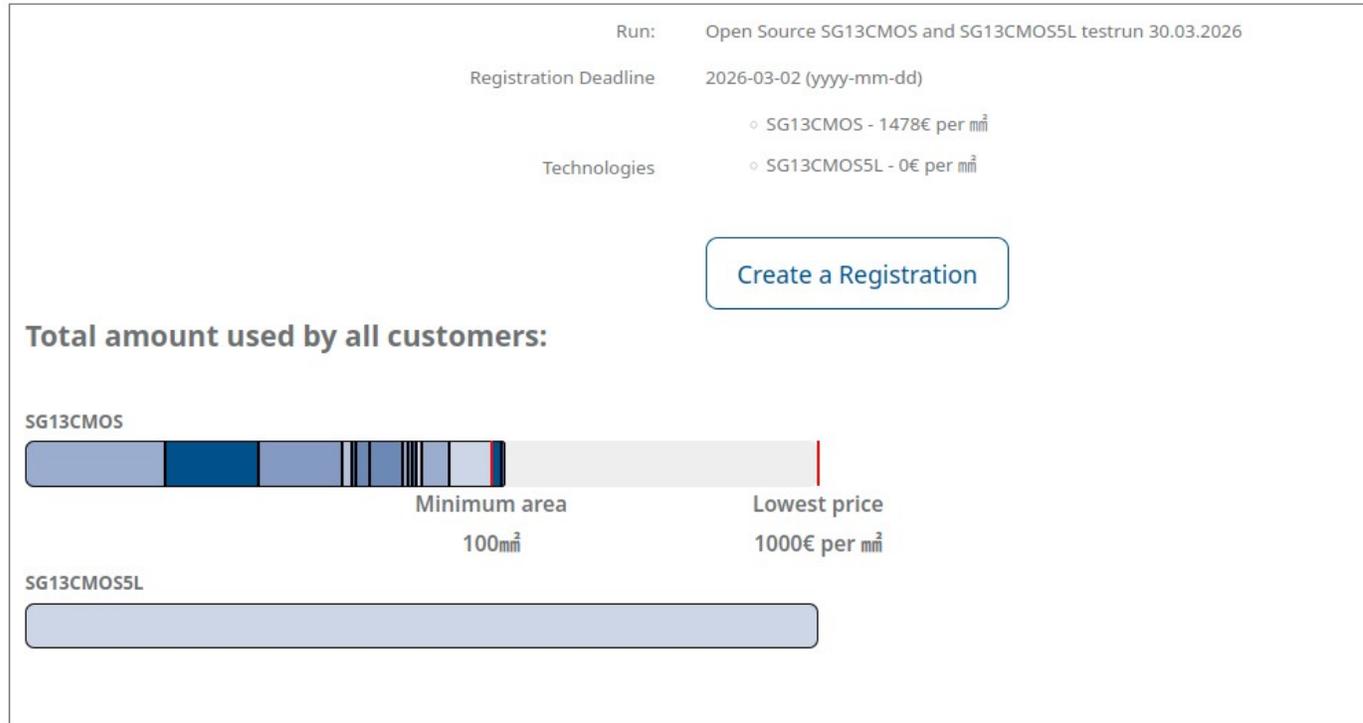
Concept to reduce costs for open-silicon MPW runs



- Usually we can sell up to 100 mm² per MPW Tape Out to customers (total area per mask set 280 mm²), but we offer **different** technologies and modules with **several** wafer lots, **several** options and wafer thicknesses
- If we have dedicated CMOS MPW runs (only SG13C technology, only one wafer lot, only one wafer thickness) with enough customers (appr. 150 mm²) we could go down with price
- To maintain OpenMPW program IHP plans 2 – 4 runs per year
 - SG13CMOS – CMOS only run with AL BEOL where price starts at 1500 €/mm² (for 100 mm²) goes down to **1000 €/mm²** depends on area request
 - By reducing layer and fabrication steps costs can be reduced to **900 €/mm²** and lower
- SG13CMOS-5L technology offered for open-source education designs and which includes front-end of SG13CMOS, but **no** isolated NMOS, further **only** 4 thin metal layer and one 2µm thick TopMetal and **no** MIM capacitor

First open-silicon MPW run March 2026 is already booked

- 2-4 open source MPW runs per year depending on user requests



MPW will only be launched if the required order limit is reached, see example for March 2026.

The price starts at € 1500 / mm² and can be reduced to € 1000 / mm² if demand is higher (1478 € 27th of February).

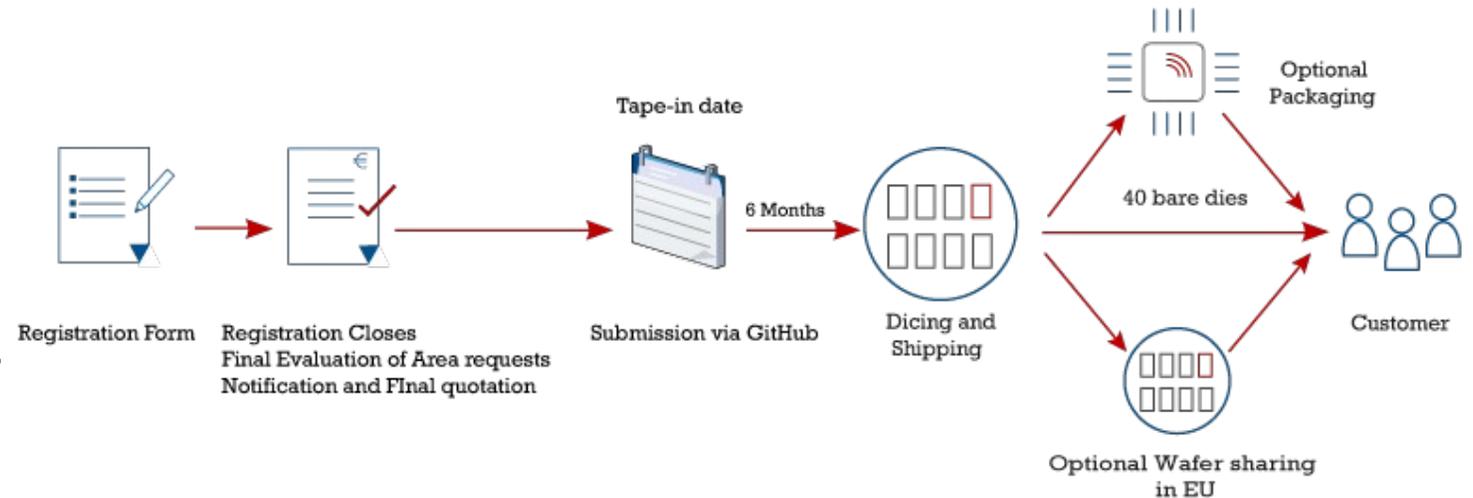
Further information:
dk.ihp-microelectronics.com/OpenSourceRequest.php

- All design data and silicon samples will be available as open source
- CMOS-5L will bring further cost reduction

Open-silicon MPW upcoming Flow



- 0 The mentioned prices refer to the open-source designs, where all the views are compatible with the open source EDA tools - upload via Github repository mandatory
- 0 For disclosed designs/IP, we offer participation OpenMPW program at a 20% discount, as the **wafers can be shared** with other users with EU – user need to sign an agreement
- 0 The typical offer includes 40 bare die samples with 200µm thickness only, up to **500 samples** are possible.
- 0 A low cost **QFN Packaging** offer is in preparation for 2026





Open Silicon MPW Program Participation Agreement

- Design data under this MPW program must be released to the public under the Apache License, Version 2.0 on dedicated Github repository of IHP
- Participant agrees to:
 - Document and publish **all post-silicon measurement data and evaluation results**
 - This includes clear measurement procedures, test setups, test software and scripts
- One year after shipment of first silicon samples to the participant, **samples available for open-source community** (open-hardware concept)
- Add. Publication, support and **export** regulations

Check details under: https://dk.ihp-microelectronics.com/includes/Open-source_MPW_shuttle_agreement.pdf

IHP Open Source Roadmap / Projects



DE:Sign – Design tools for sovereign chip development with open source:

- DI-Flowspace (16ME0986k) – **Radiation Hard** Open Source PDK
- DI-DEMICO (16ME0944) – Advanced **Open Source RF Designs**, improvement of openEMS EM simulator
- DI-SIGN-HEP (16KIS2067K) – SRAM generator, OTP, RRAM
- DI-OCDCpro (16ME0940) – **Student Design challenge** on secure designs

European projects:

- APECS pilot line – Development of an open source interposer ADK
- DECIDE – Integration of open source offerings (PDKs, EDA tools, Design IP, design trainings) in **EU chips design platform** - <https://eurocdp.eu>
- ODE4EC - Open Design Environment for European Chips – Development of analog mixed signal **EDA tools and PDKs for product development**

Analog Certificate Course



- **Course is using IHP SG13G2 Open-Source PDK**
<https://github.com/IHP-GmbH/IHP-Open-PDK>
- **Development and first run in May 19–23, 2025 within FMD-QNC project**
 - 16 on-site participants selected from 80+ applicants
 - **Feedback phase** during the course and improvement structure and content
- **Next iteration in February 23-27 at FhG IIS in Erlangen, Germany**
 - **Registration:**
<https://www.ihp-microelectronics.com/de/veranstaltungen/detail/title-certificate-course-in-person-analog-design-with-ihp-sg13g2-open-source-pdk>



Acknowledgment



- Special thanks to the following public founded German projects:
 - VE-HEP (16KIS1339K), IHP Open130-G2 (16ME0852), FMD-QNC (16ME0831)

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